

# Compal Confidential

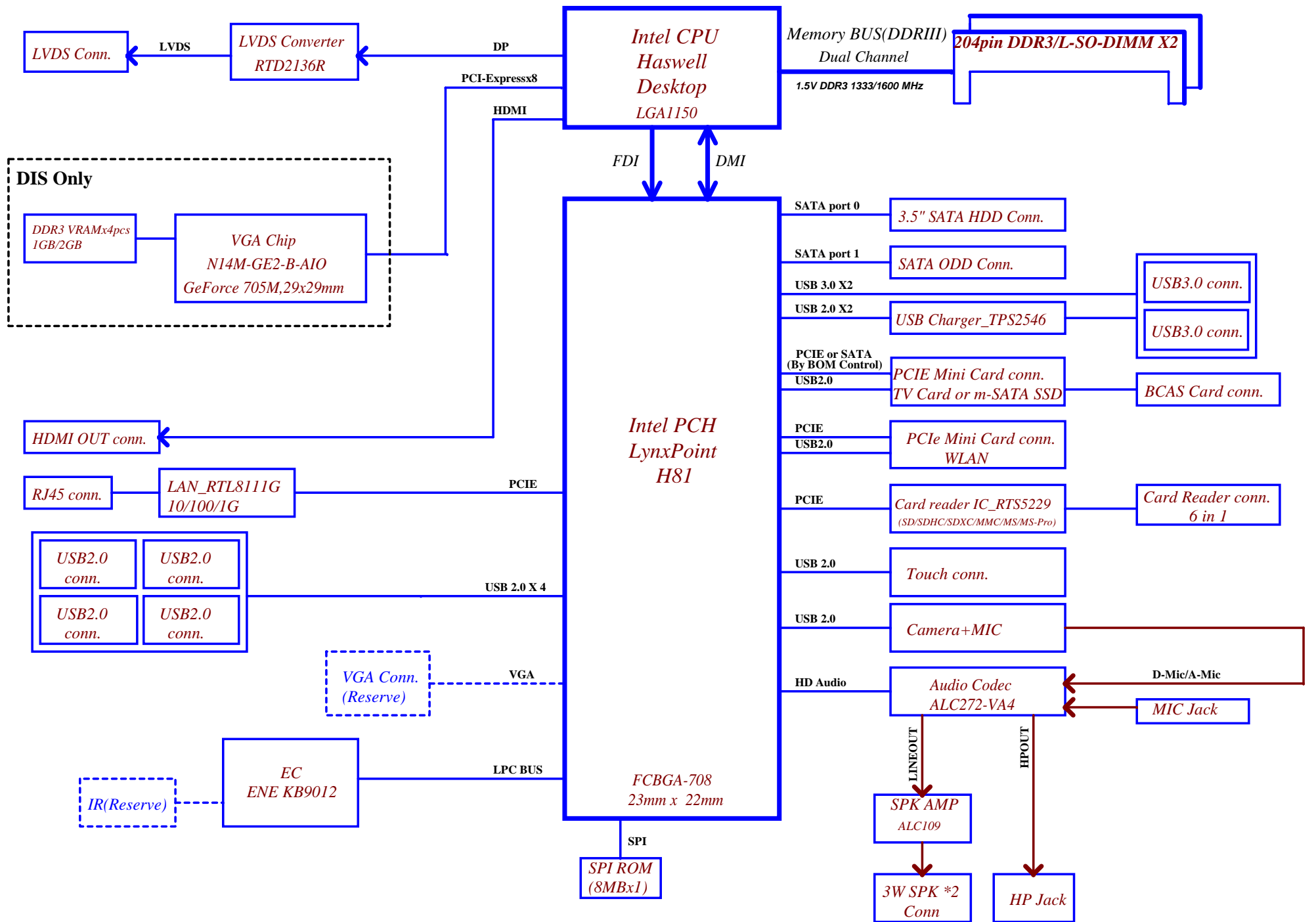
## C560 LA-A061P Schematics Document

INTEL Haswell CPU with DDRIII + PCH Lynx-Point  
AIO M/B

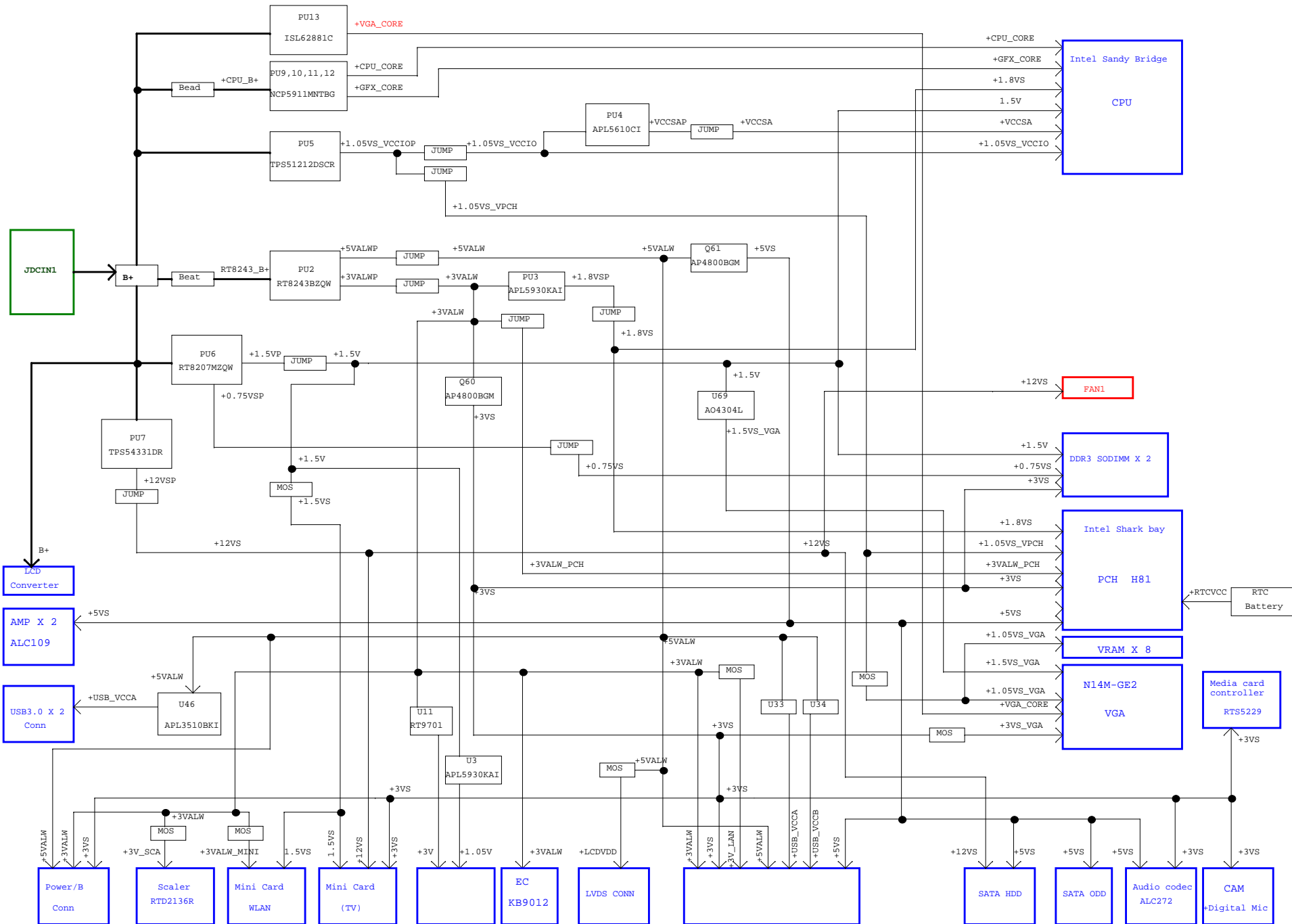
September 24, 2013

REV:1.0

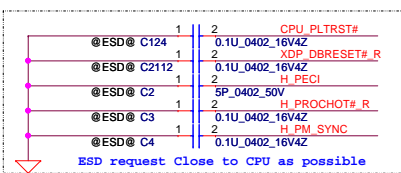
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PECI 10mil spacing and Max Length < 15"

R11 follow CDB R42PR add 0ohm serial resistor

R12 follow CDB R34PR add 0ohm serial resistor

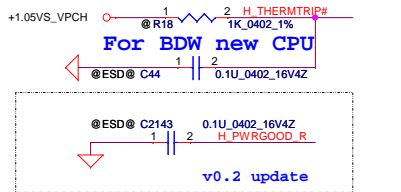
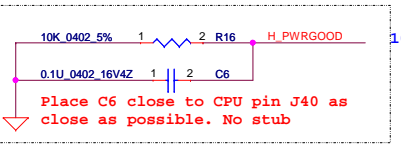
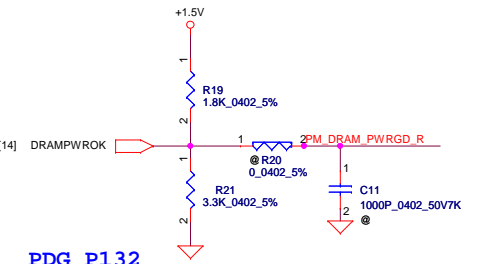


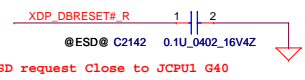
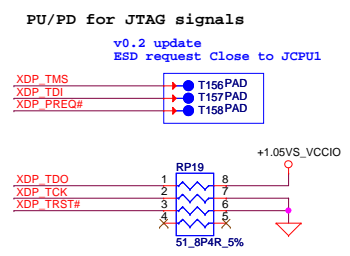
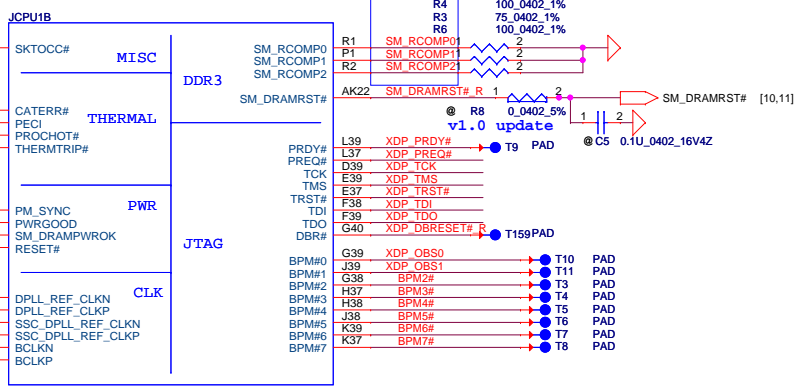
Table B-1. Configuration-wise Mapping of HDMI signals for Processor on DDI ports			
Port	Digital Display Interface (Processor Side)	HDMI Signals	Processor Digital Display Interface Pins
Port B	DDISB_TXB0	HDMI0_TX0_DP	DDISB_TXB0
	DDISB_TXB1	HDMI0_TX1_DP	DDISB_TXB1
	DDISB_TXB2	HDMI0_TX2_DP	DDISB_TXB2
	DDISB_TXB3	HDMI0_TX3_DP	DDISB_TXB3
	DDISB_TXB4	HDMI0_TX4_DP	DDISB_TXB4
	DDISB_TXB5	HDMI0_TX5_DP	DDISB_TXB5
	DDISB_TXB6	HDMI0_TX6_DP	DDISB_TXB6
	DDISB_TXB7	HDMI0_TX7_DP	DDISB_TXB7
	DDISB_TXB8	HDMI0_TX8_DP	DDISB_TXB8
	DDISB_TXB9	HDMI0_TX9_DP	DDISB_TXB9
Port C	DDISC_TXC0	HDMI1_TX0_DP	DDISC_TXC0
	DDISC_TXC1	HDMI1_TX1_DP	DDISC_TXC1
	DDISC_TXC2	HDMI1_TX2_DP	DDISC_TXC2
	DDISC_TXC3	HDMI1_TX3_DP	DDISC_TXC3
	DDISC_TXC4	HDMI1_TX4_DP	DDISC_TXC4
	DDISC_TXC5	HDMI1_TX5_DP	DDISC_TXC5
	DDISC_TXC6	HDMI1_TX6_DP	DDISC_TXC6
	DDISC_TXC7	HDMI1_TX7_DP	DDISC_TXC7
	DDISC_TXC8	HDMI1_TX8_DP	DDISC_TXC8
	DDISC_TXC9	HDMI1_TX9_DP	DDISC_TXC9
Port D	DDID_TXD0	HDMI2_TX0_DP	DDID_TXD0
	DDID_TXD1	HDMI2_TX1_DP	DDID_TXD1
	DDID_TXD2	HDMI2_TX2_DP	DDID_TXD2
	DDID_TXD3	HDMI2_TX3_DP	DDID_TXD3
	DDID_TXD4	HDMI2_TX4_DP	DDID_TXD4
	DDID_TXD5	HDMI2_TX5_DP	DDID_TXD5
	DDID_TXD6	HDMI2_TX6_DP	DDID_TXD6
	DDID_TXD7	HDMI2_TX7_DP	DDID_TXD7
	DDID_TXD8	HDMI2_TX8_DP	DDID_TXD8
	DDID_TXD9	HDMI2_TX9_DP	DDID_TXD9



PDG P132

HSW A0+LPT A0 change R21to 4.7K, R19 to 3.3K

Trace width=12mil, spacing 20mil, max L=500mil



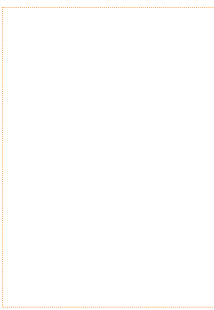
DP\_RCOMP trace width=20mil spacing 25mil length<200mil

FDI For VGA

eDP brightness

eDP

(To LVDS Converter)

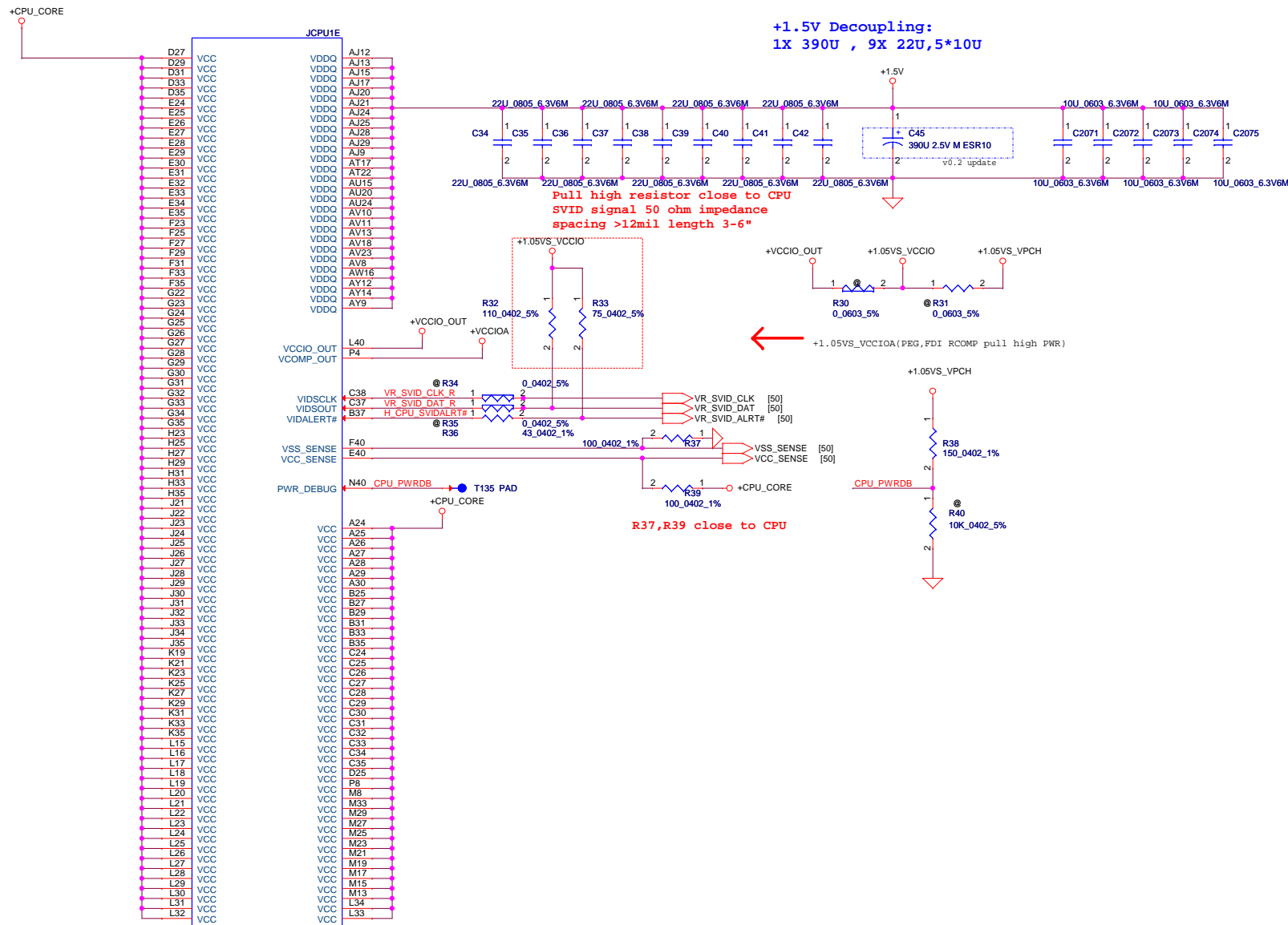


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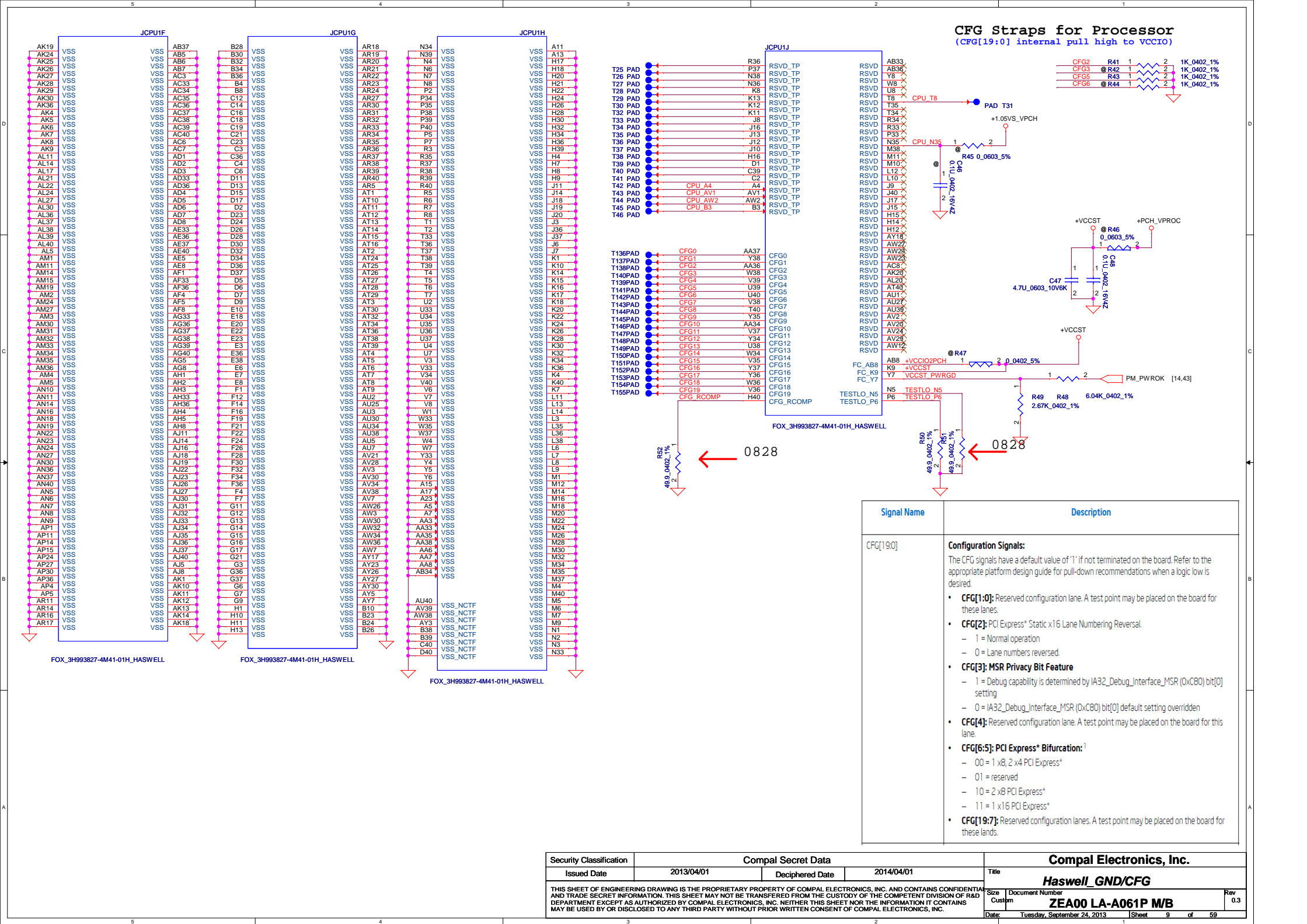




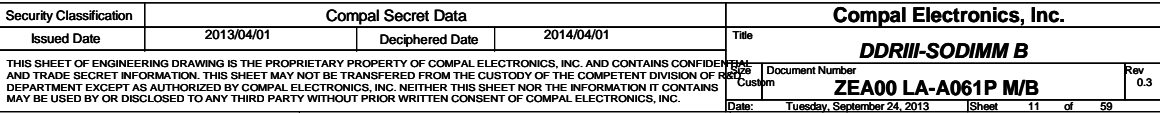
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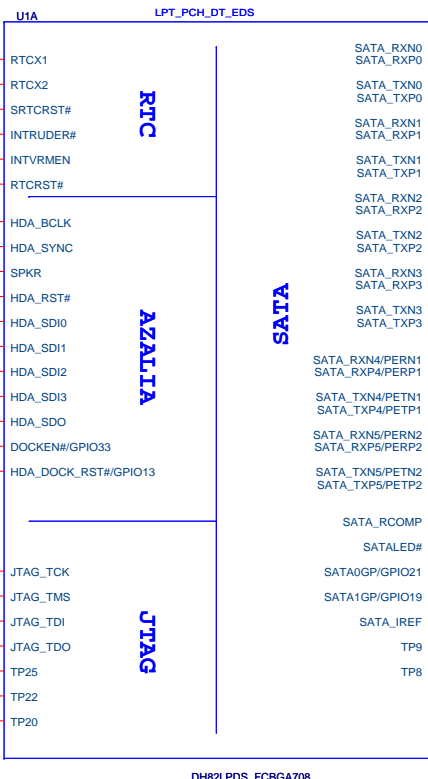
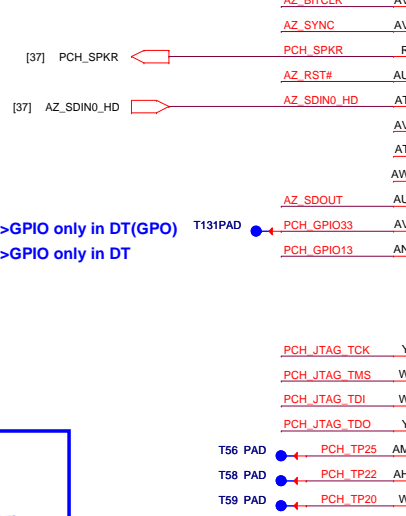
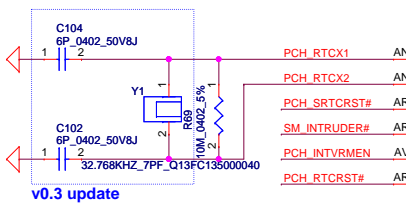
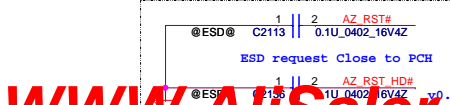
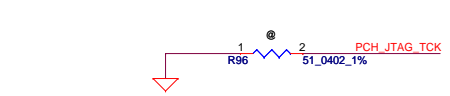
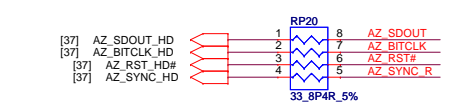
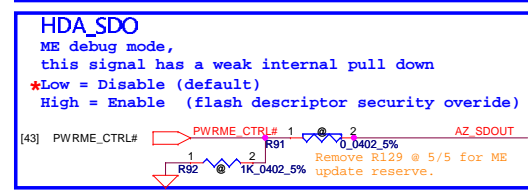
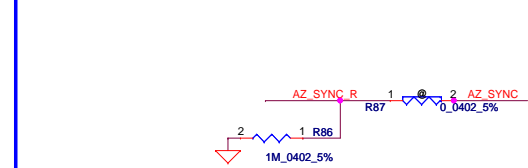
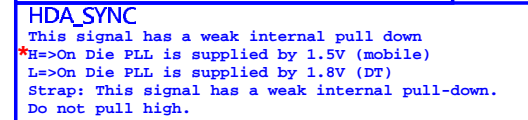
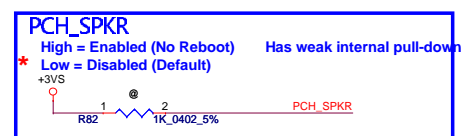
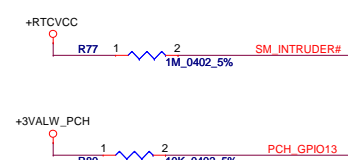
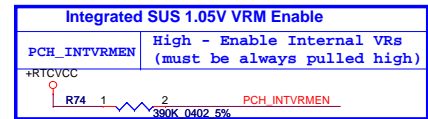
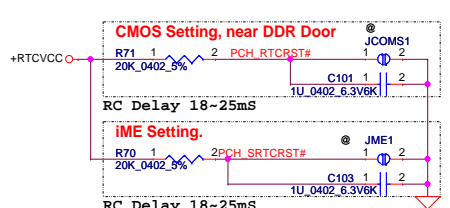
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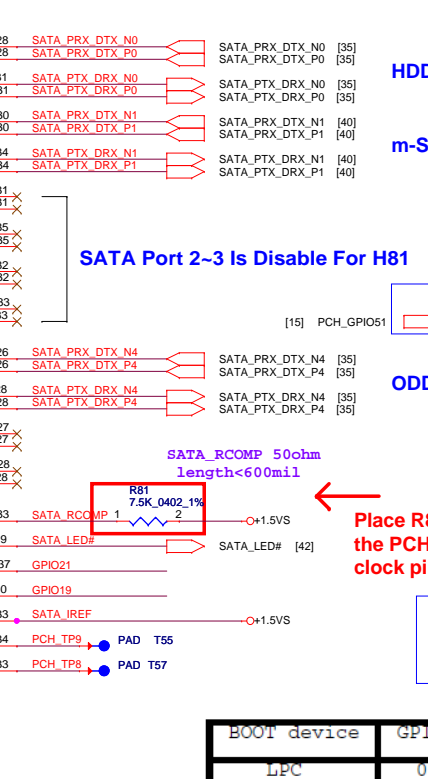




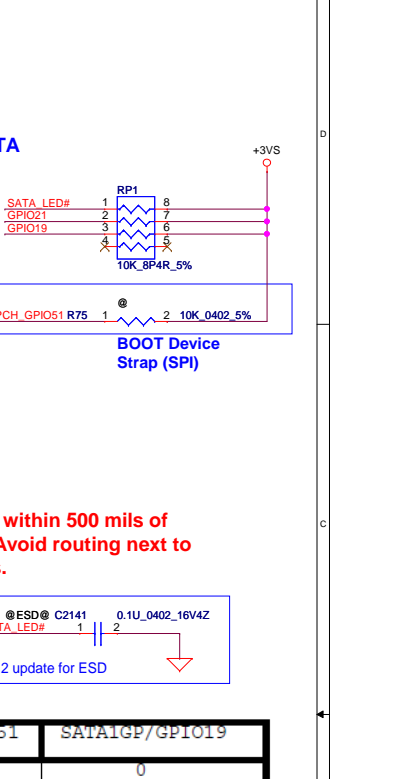
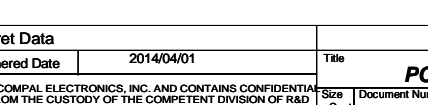
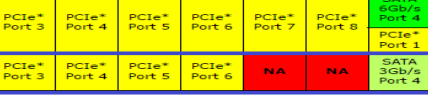
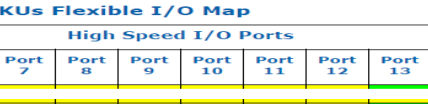
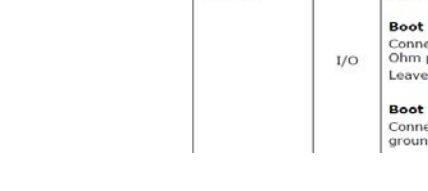
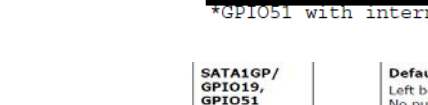




DH82LPDS\_FCBGA708



Place R81 within 500 mils of the PCH. Avoid routing next to clock pins.



BOOT Device Strap (SPI)

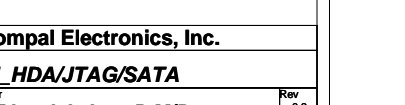
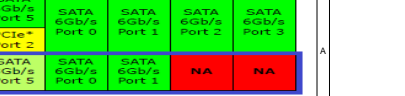
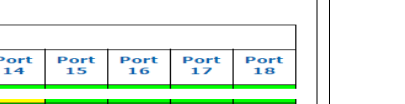
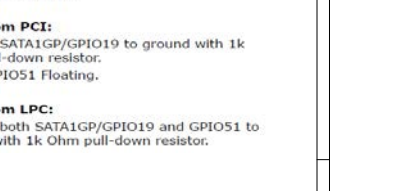
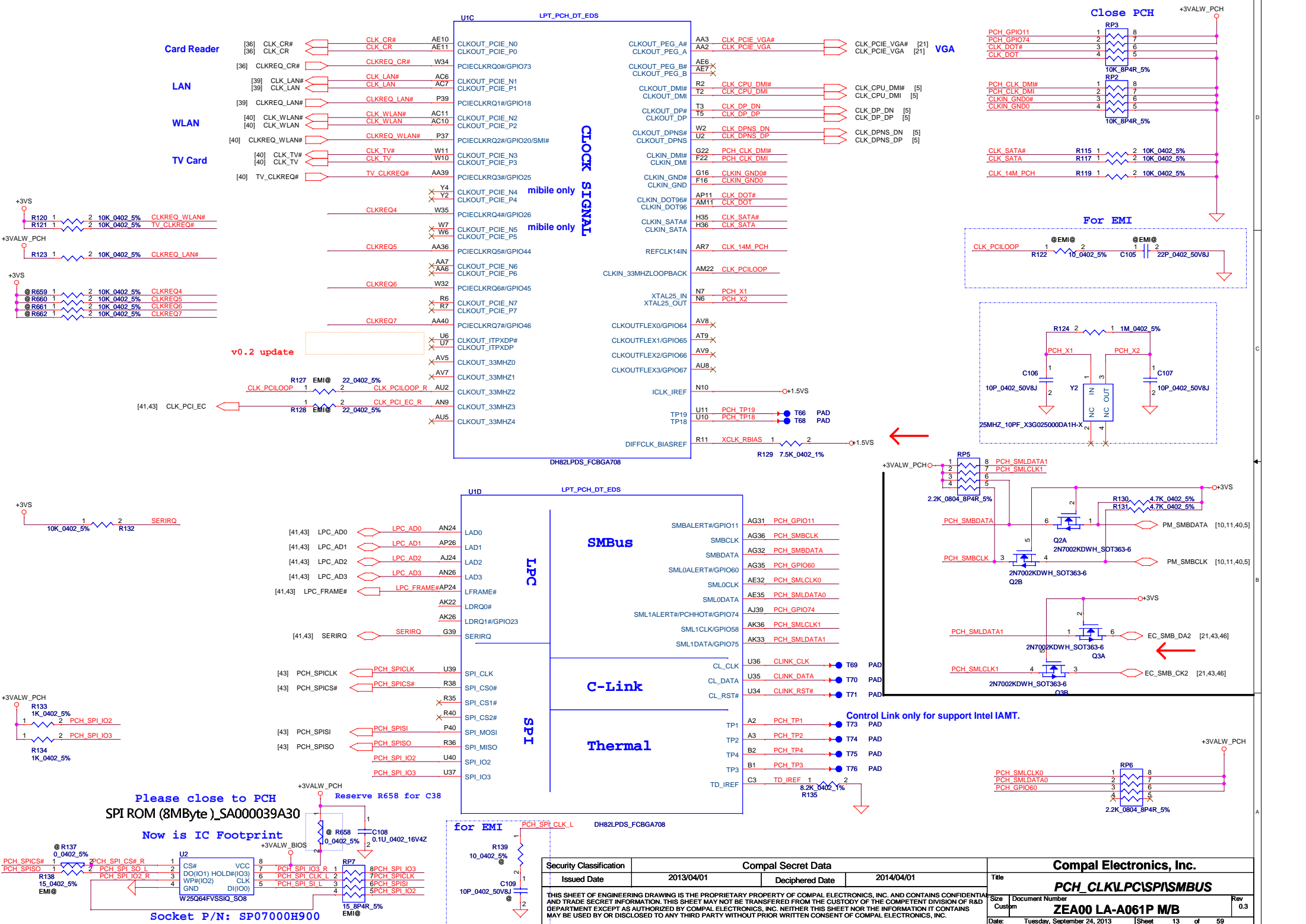


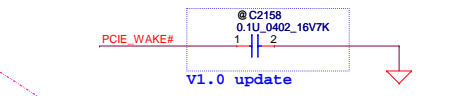
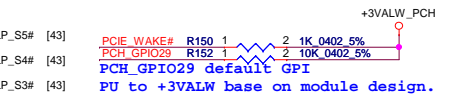
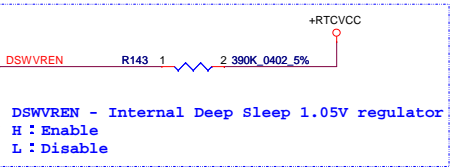
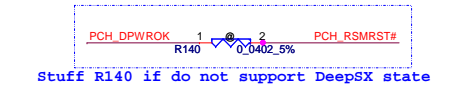
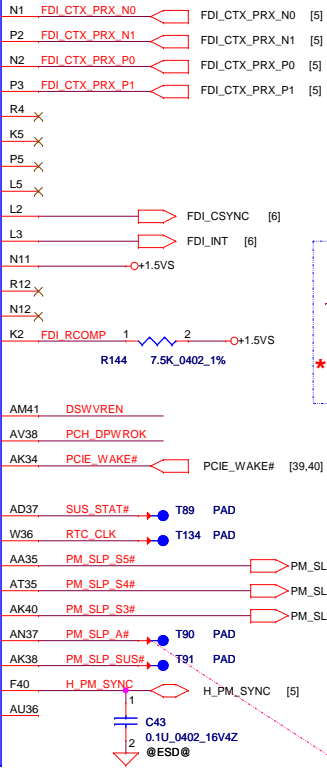
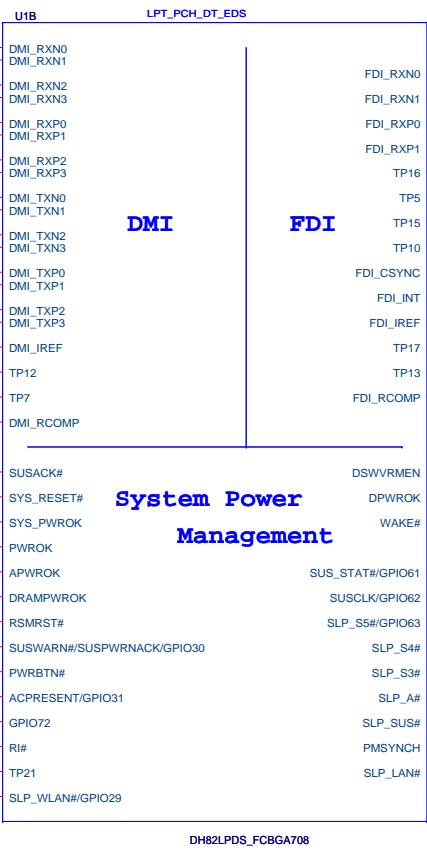
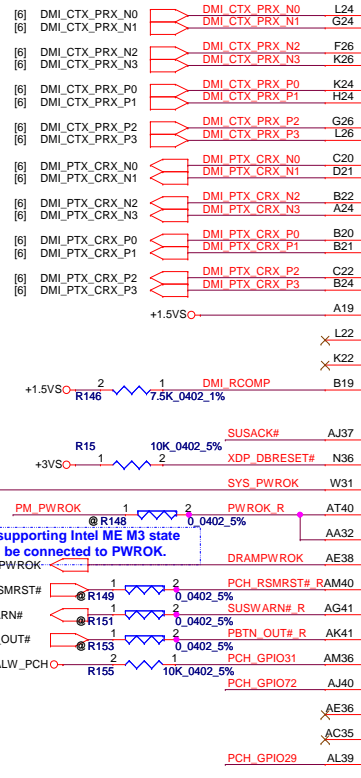
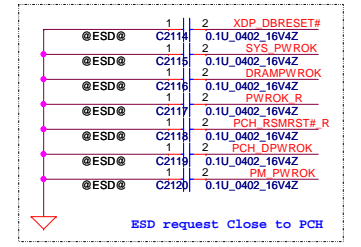
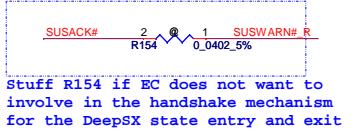
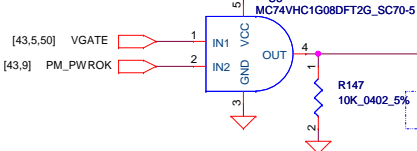
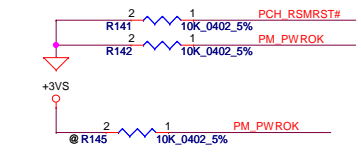
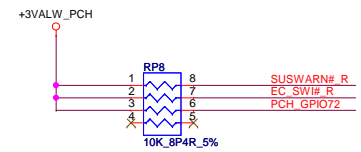
Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 7	USB 3.0 Port 8	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	NA	NA	NA	NA	NA	NA

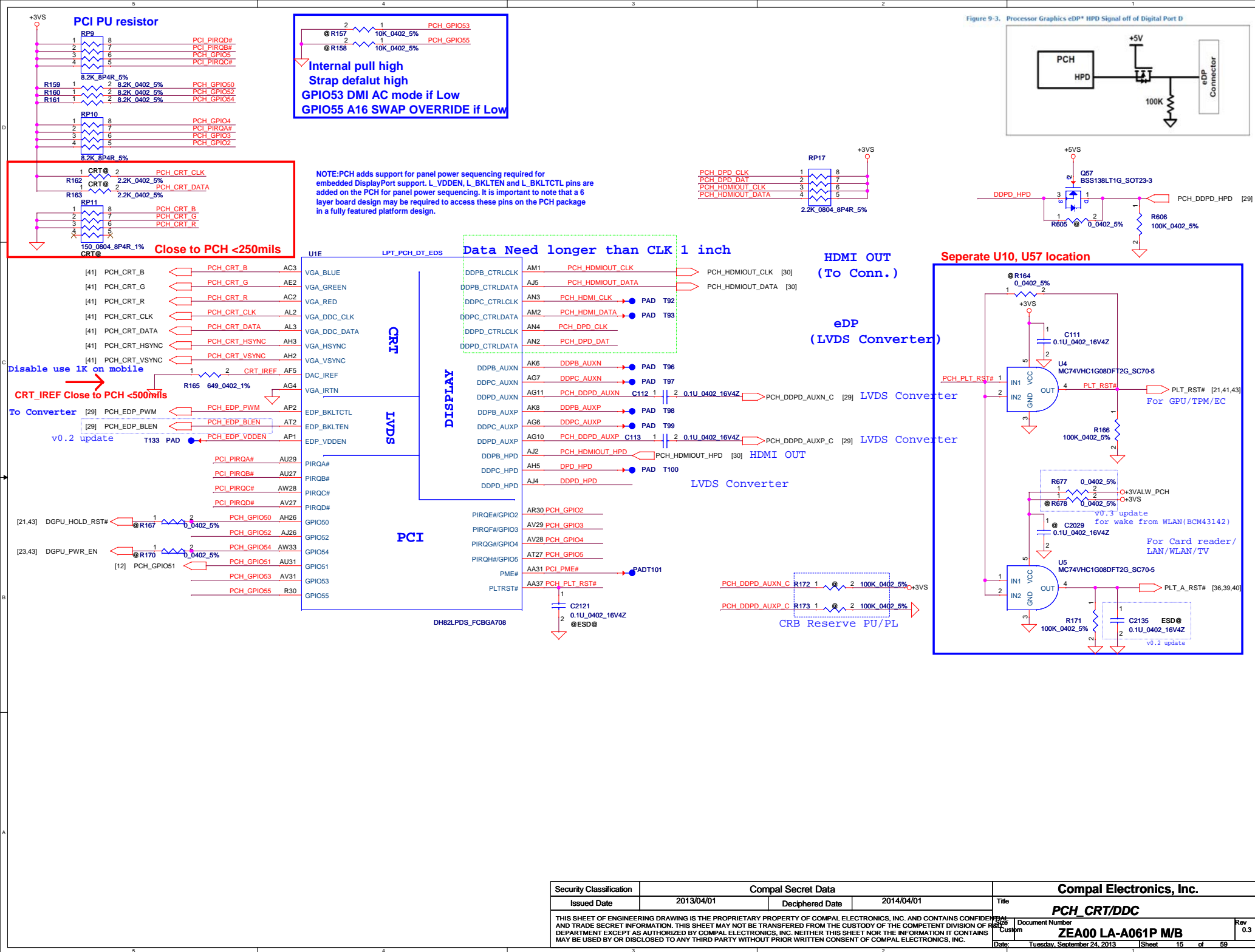
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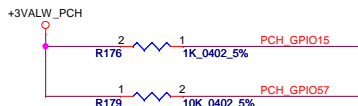


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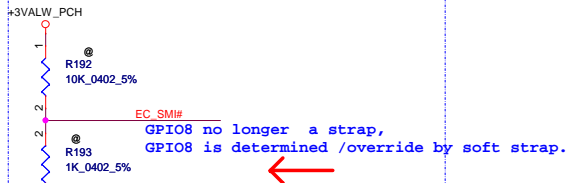


#### GPIO8

Integrated Clock Chip Enable (Removed)

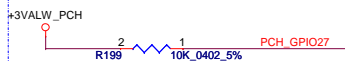
H: Disable

L: Enable



This signal has a weak internal pull-up but requires an external pull down.

The current default is clock enable



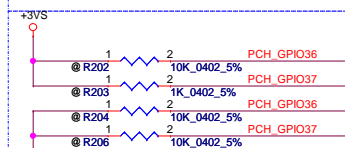
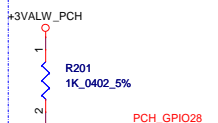
In Deep Sleep Power Well. Unmuxed. Defaults to GPI. Not used Weak pull-up 10kΩ to VccDSW3\_3 -->Check list1.5 P402. PD to GND for Huron River!!

#### GPIO28

On-Die PLL Voltage Regulator

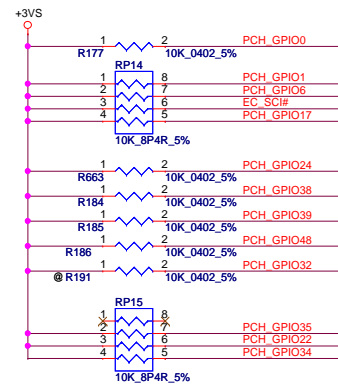
H: Enable

L: Disable



Clock validation strap  
ICG is EN when LOW  
\*GPIO36 with internal pull-down

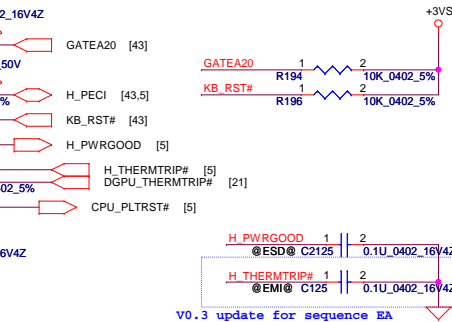
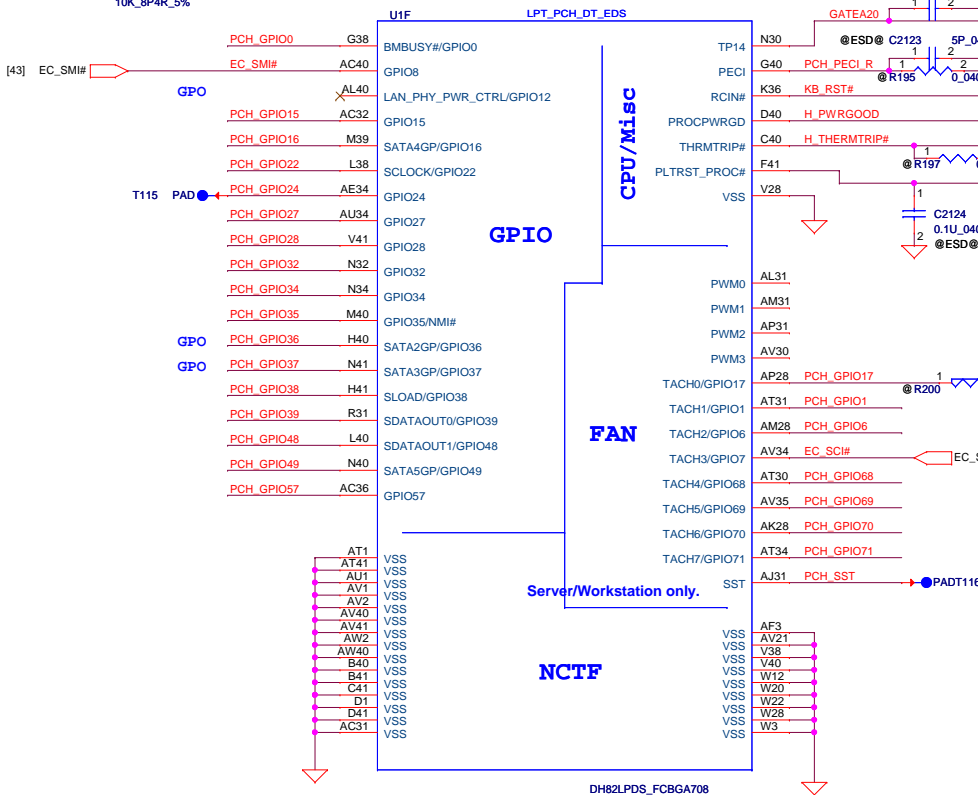
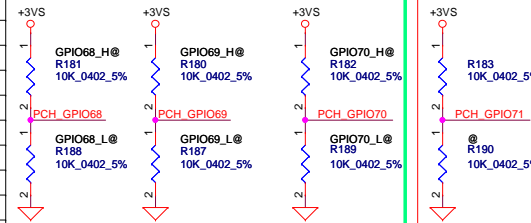
TLs  
Hi:with confidentiality  
Low:with no confidentiality  
\*GPIO37 with internal pull-down



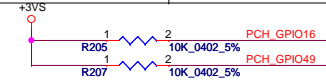
120821

SKU ID	GPIO68	GPIO69	GPIO69
SKU1	0	0	0
SKU2	0	0	1
SKU3	0	1	0
SKU4	0	1	1
SKU5	1	0	0
SKU6	1	0	1
SKU7	1	1	0
SKU8	1	1	1

#### SKU ID TABLE



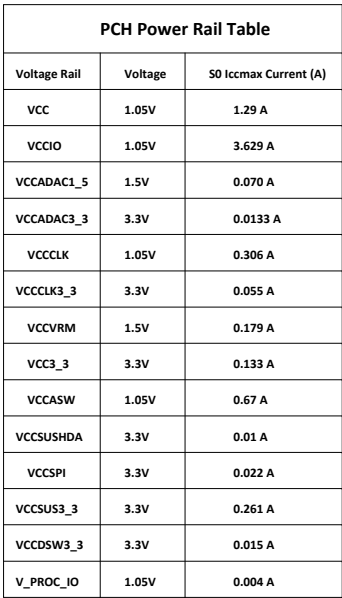
Config	PCHSTRAP 4&9
Set by GPIO16/49	11
USB X6,PCIEX8,SATAx4	01
USB X4,PCIEX8,SATAx6	00



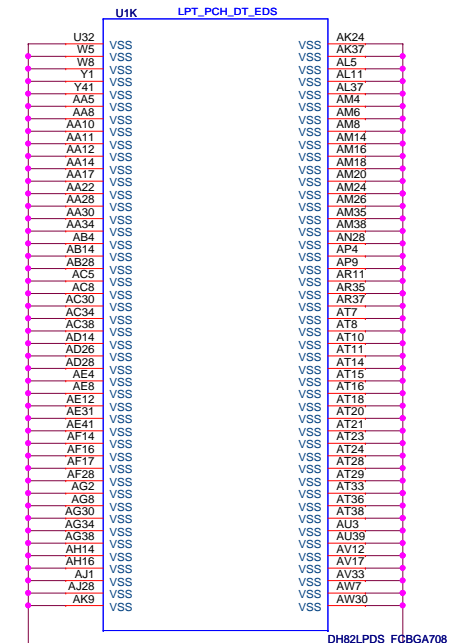
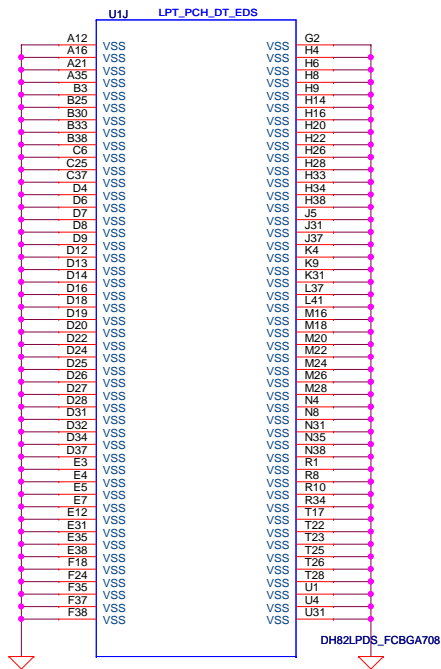
Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)							(00)	(00)				
				USB3 3	USB3 4							PCIE 1	PCIE 2				
				(01)	(01)							(01)	(01)				

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								PCH_CPU/GPIO	
								ZEA00 LA-A061P M/B	
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								Date: Tuesday, September 24, 2013	
								Sheet 17 of 59	



[illegible]

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



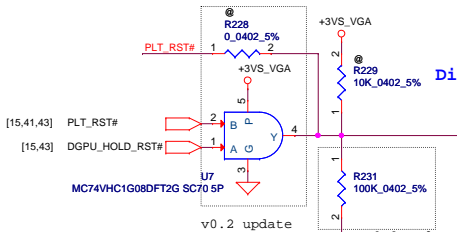
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[6] PCIE\_CTX\_C\_GRX\_P0[0..15] PCIE\_CTX\_C\_GRX\_P0[0..15]  
[6] PCIE\_CTX\_C\_GRX\_N0[0..15] PCIE\_CTX\_C\_GRX\_N0[0..15]  
[6] PCIE\_CTX\_C\_GRX\_P0[0..15] PCIE\_CTX\_C\_GRX\_P0[0..15]  
[6] PCIE\_CTX\_C\_GRX\_N0[0..15] PCIE\_CTX\_C\_GRX\_N0[0..15]

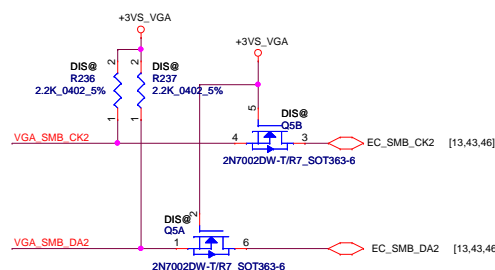
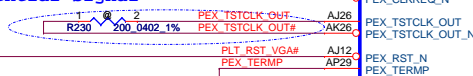
Reserve for x16 GPU

PCIE\_CTX\_C\_GRX\_P0 AK12 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P1 AK13 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P2 AK14 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P3 AK15 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P4 AK16 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P5 AK17 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P6 AK18 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P7 AK19 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P8 AK20 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P9 AK21 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P10 AK22 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P11 AK23 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P12 AK24 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P13 AK25 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P14 AK26 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_P15 AK27 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_N0 AK12 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_N1 AK13 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_N2 AK14 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_N3 AK15 PEX\_RX0\_N  
PCIE\_CTX\_C\_GRX\_N4 AK16 PEX\_RX0\_N  
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PCIE\_CTX\_C\_GRX\_N7 AK19 PEX\_RX0\_N  
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Reserve for x16 GPU

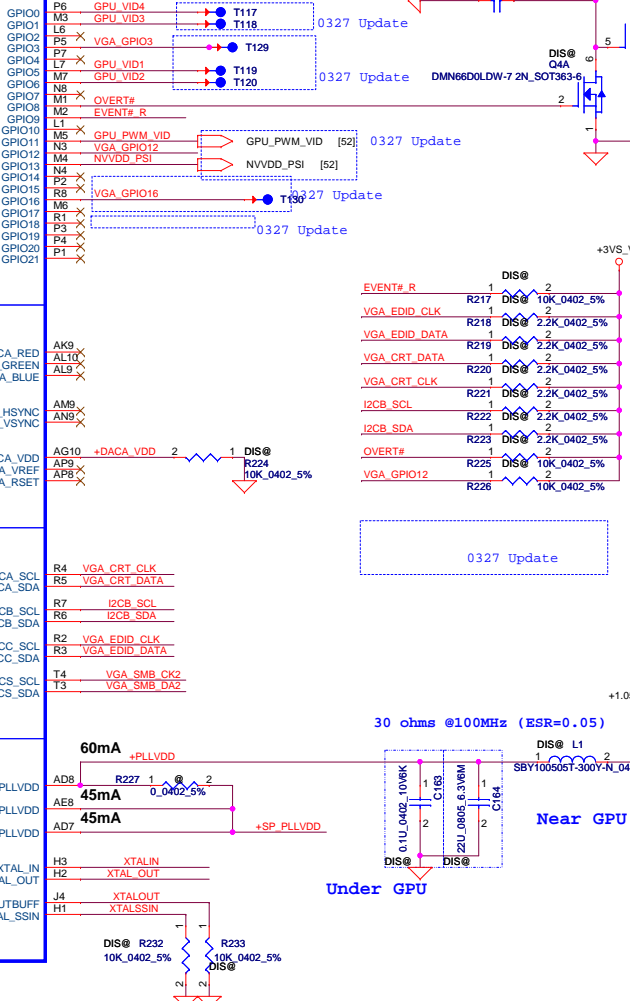


Differential signal



Reserve pull-up and down.  
Don't have to install  
component for default, NV  
reply on 5/4. when system  
no support CLKREQ

Part 1 of 7  
GPIO  
DACs  
PCIEXPRESS  
I2C  
CLK



30 ohms @100MHz (ESR=0.05)

Near GPU

Under GPU

Table 02. GB2-64 and GB4-128 GPIO Description

GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	0	GPU Core VDD VID4	Strap to boot INVDD
GPIO1	GPU_VID3	0	GPU Core VDD VID3	Strap to boot INVDD
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	0	Panel Power Enable or Phase Shedding	LCD_VCC: 100K pull-down; PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEI	0	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	0	GPU Core VDD VID1	Strap to boot INVDD
GPIO6	GPU_VID2	0	GPU Core VDD VID2	Strap to boot INVDD
GPIO7	3D_Vision	0	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	0	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	0	GPU Core VDD VID0	Strap to boot INVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	0	GPU Core VDD VID5	Strap to boot INVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	0	Phase Shedding or Memory VDD VID	PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default; MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

Under GPU(below 150mils)  
Put C169 close to U65.AE8

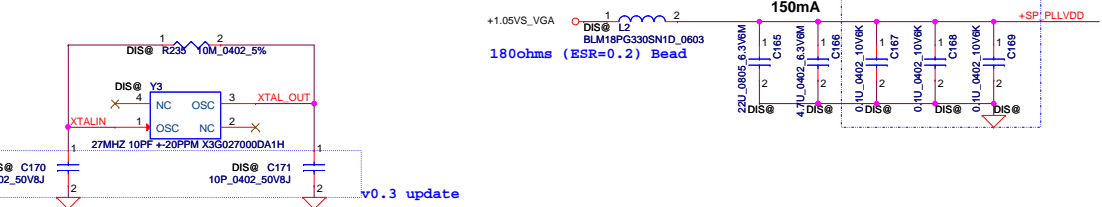
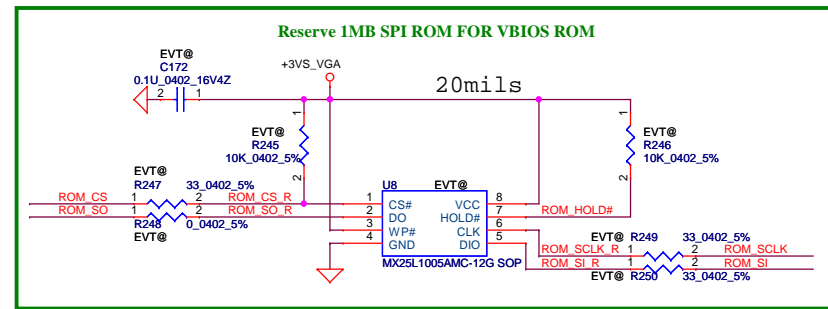
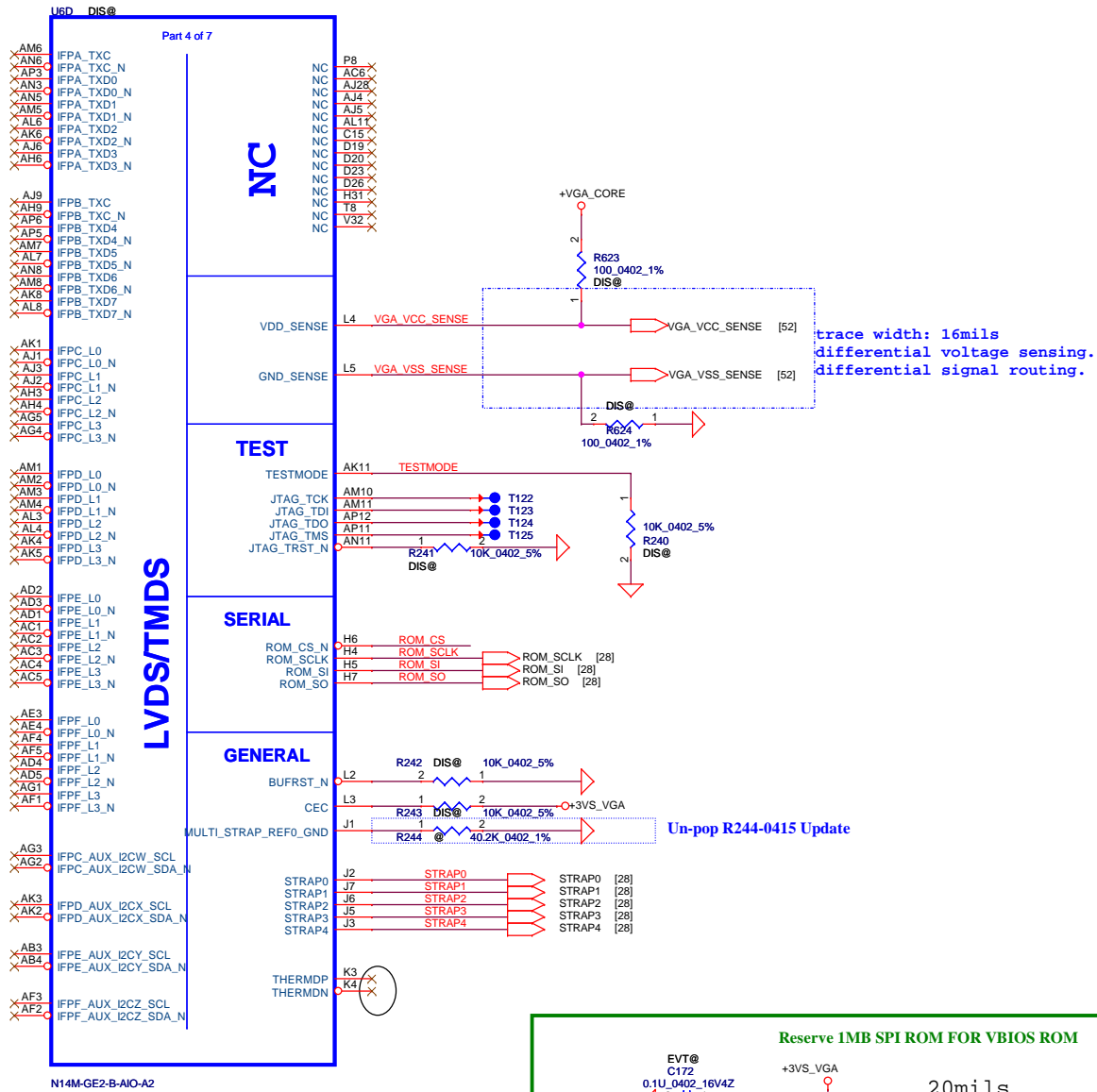




Table 66. N13x Family Display Link Summary

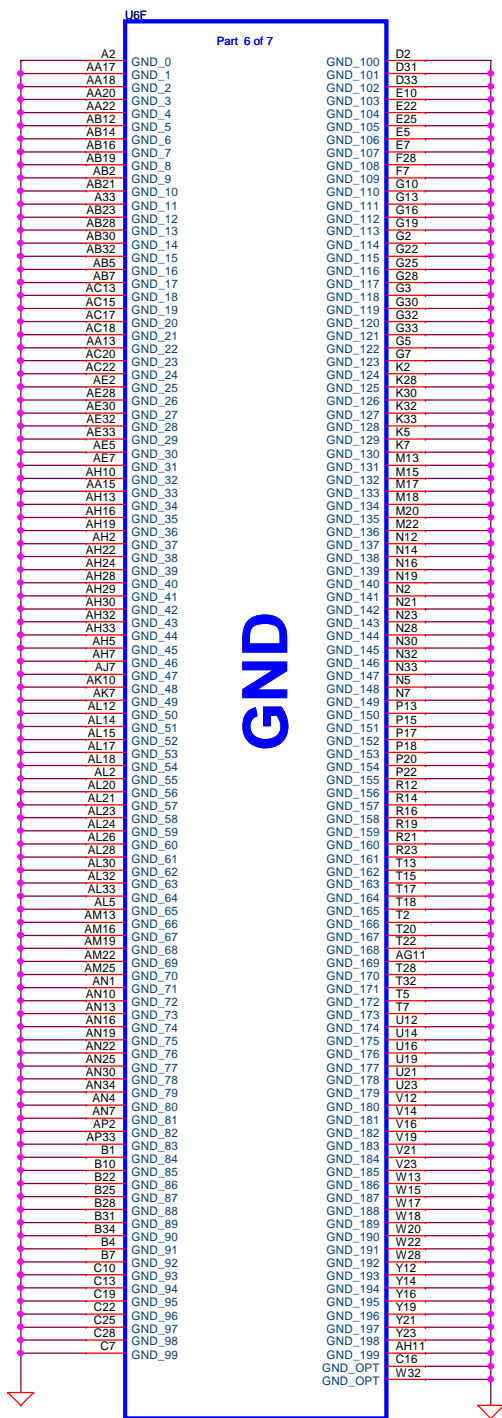
Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI



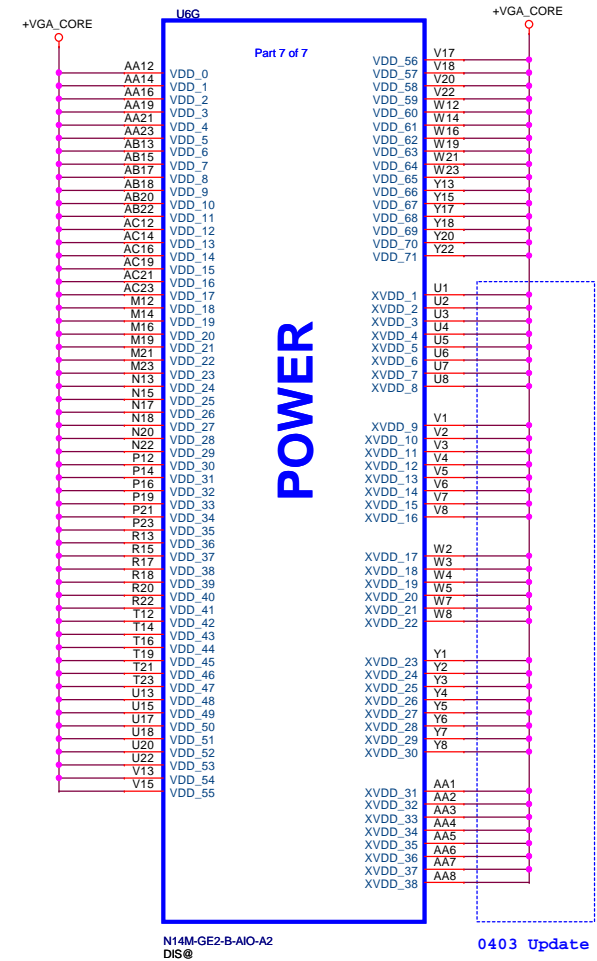
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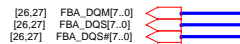
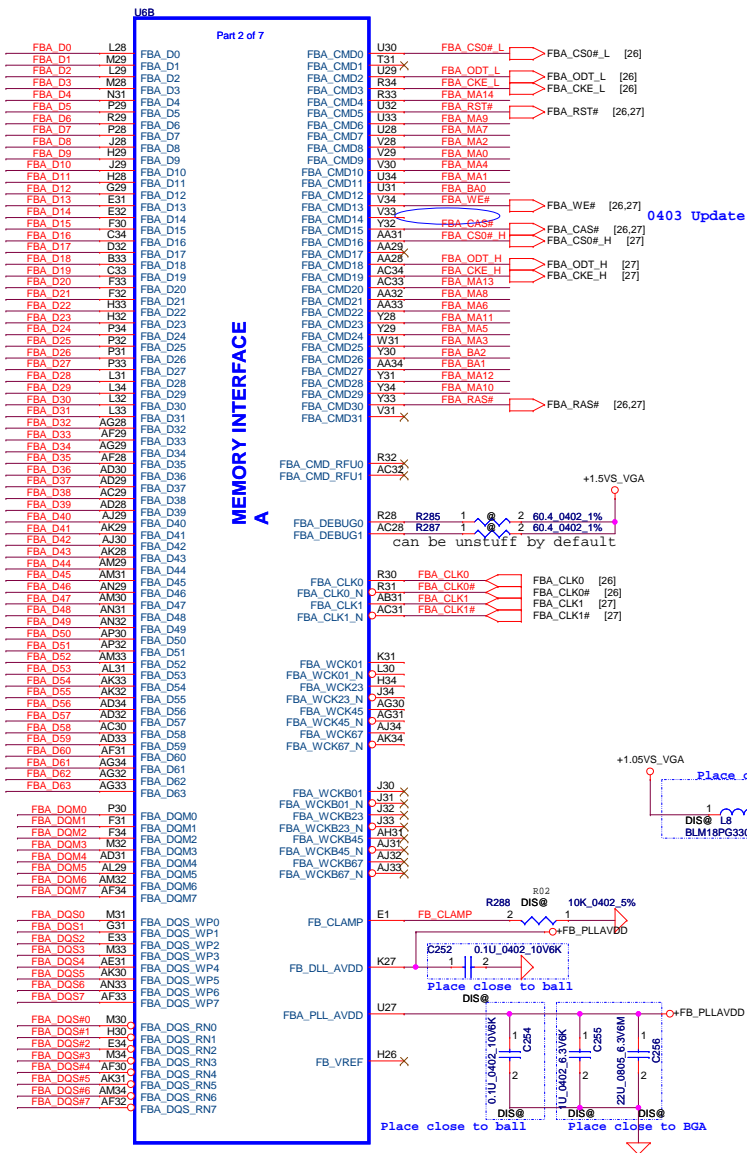
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DIS@



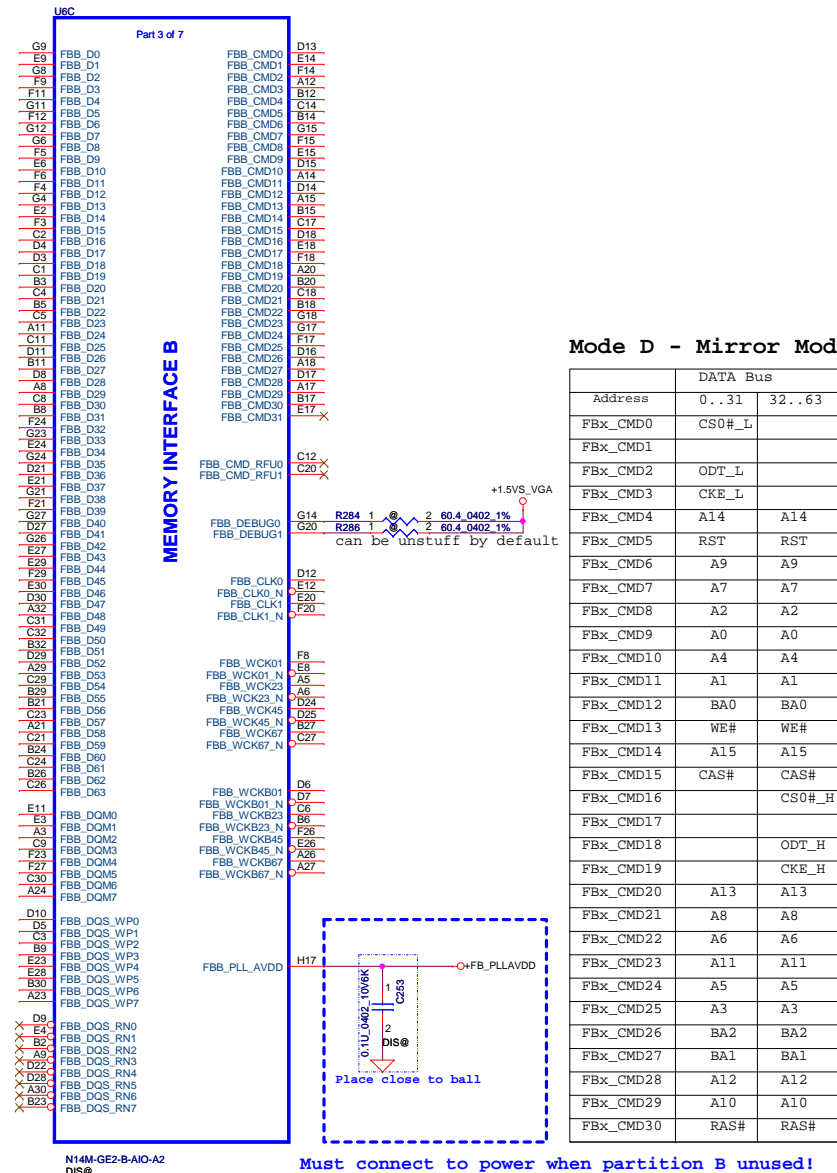
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DIS@

0403 Update

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						Size		Document Number		Rev	
								<b>ZEA00 LA-A061P M/B</b>		<b>0.3</b>	
						Date:		Tuesday, September 24, 2013		Sheet 24 of 59	



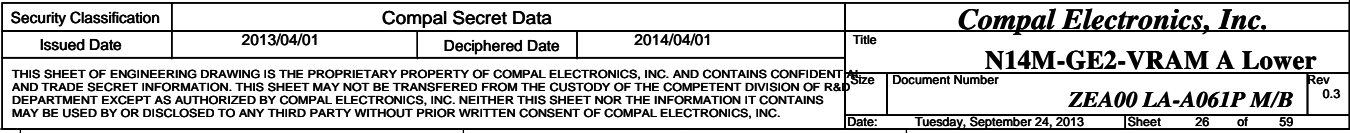
30ohms (ESR=0.01) Bead  
P/N:SM010007W00



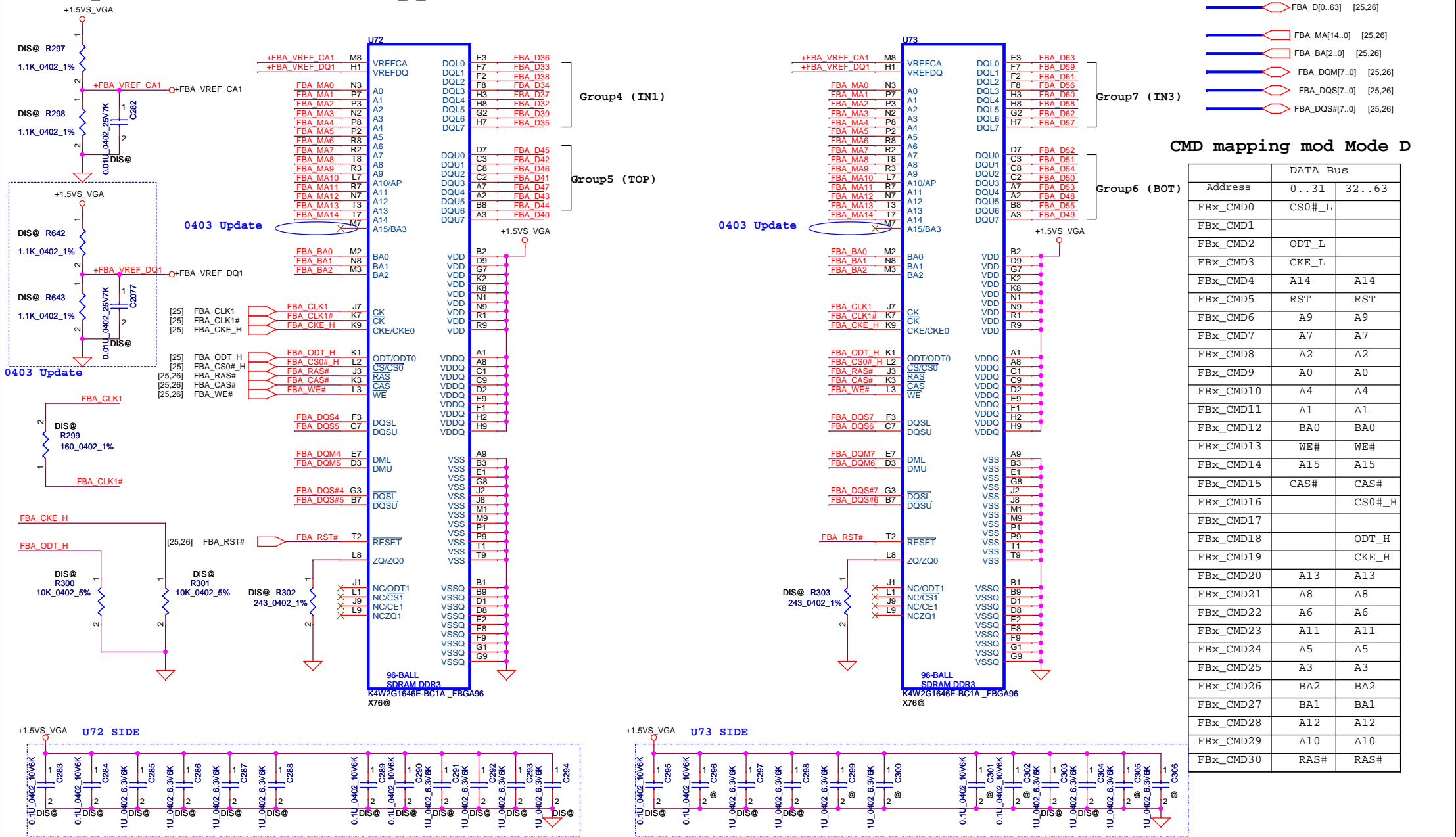
### Mode D - Mirror Mode Mapping

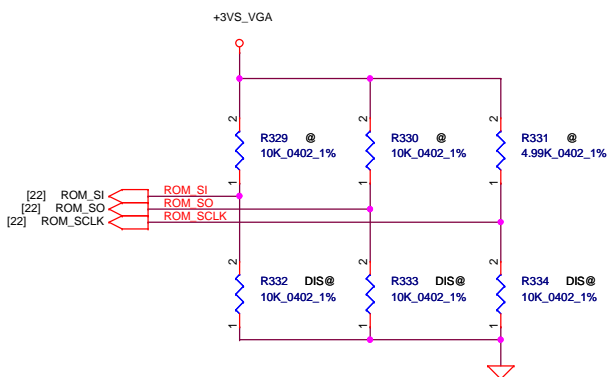
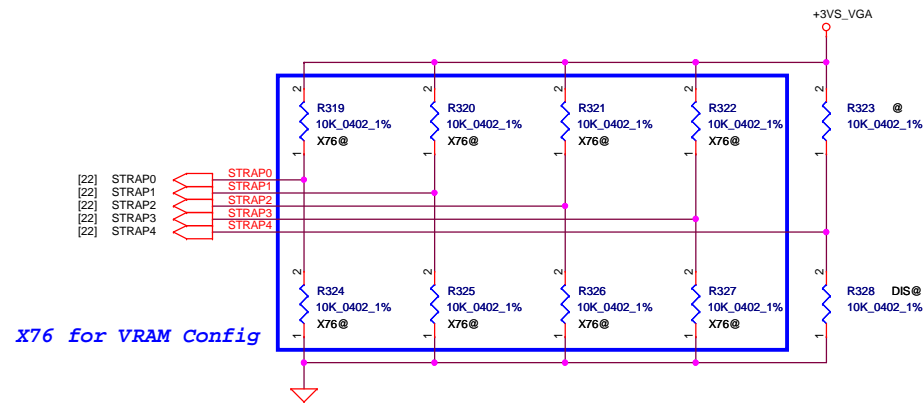
Address		DATA Bus	
0..31		32..63	
FBx_CMD0	CS0#_L		
FBx_CMD1			
FBx_CMD2	ODT_L		
FBx_CMD3	CKE_L		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE#	WE#	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16	CS0#_H		
FBx_CMD17			
FBx_CMD18	ODT_H		
FBx_CMD19	CKE_H		
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	

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Memory Partition A - Upper 32 bits





[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k $\Omega$	Pull-down to GND
ROM_SI	SUB_VENDOR	10k $\Omega$	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k $\Omega$	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k $\Omega$	See Note
STRAP1	RAM_CFG[1]	10k $\Omega$	See Note
STRAP2	RAM_CFG[2]	10k $\Omega$	See Note
STRAP3	RAM_CFG[3]	10k $\Omega$	See Note
STRAP4	PCIE_MAX_SPEED	10k $\Omega$	Pull-down to GND

[VRAM Config-RVL-06366-001]

GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G-K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G-E SA000065D20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AFR-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

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								Size		Document Number		Rev	
										ZEA00 LA-A061P M/B		0.3	
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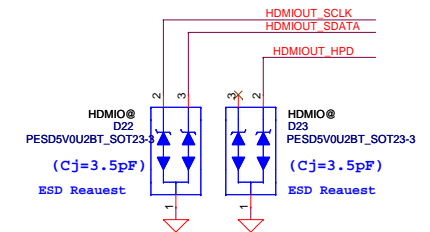
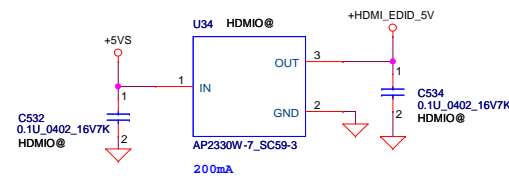
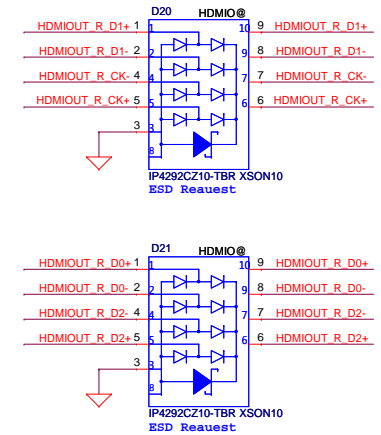
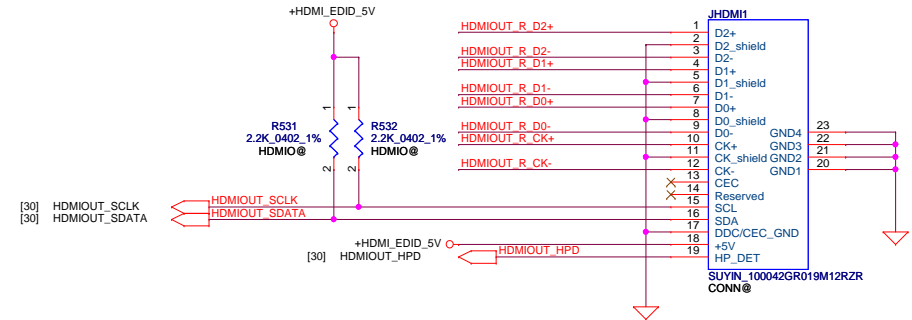
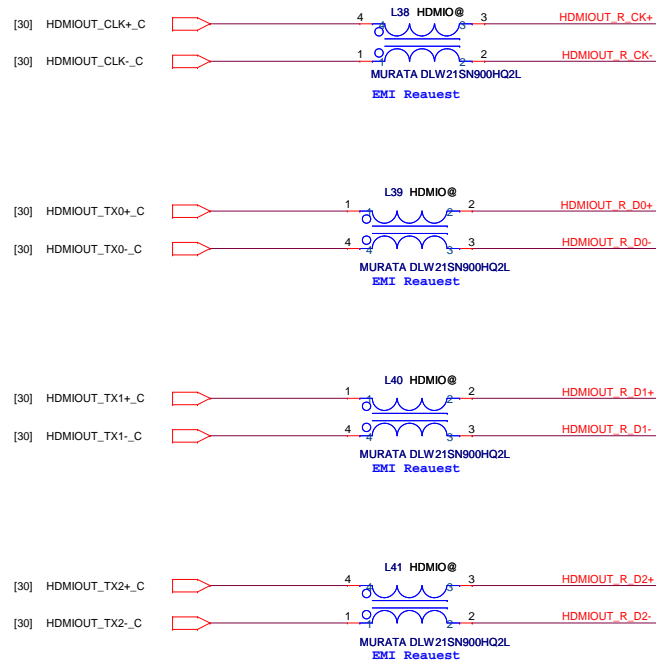




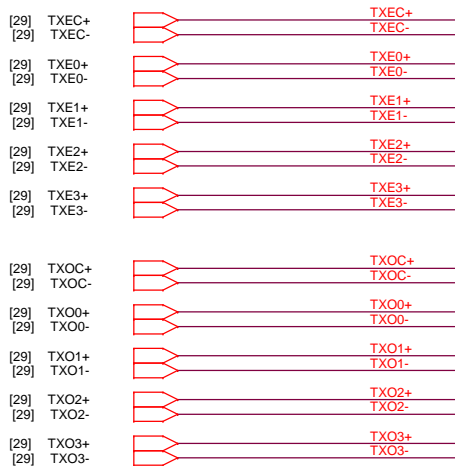




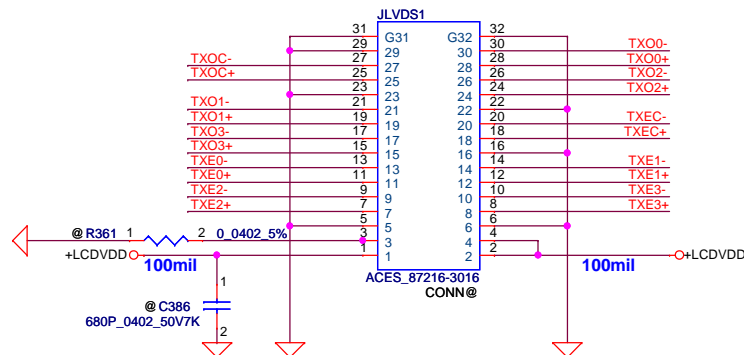
## HDMI-OUT Connector



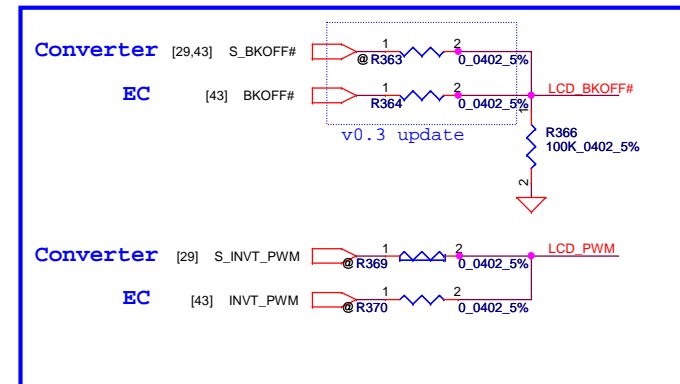
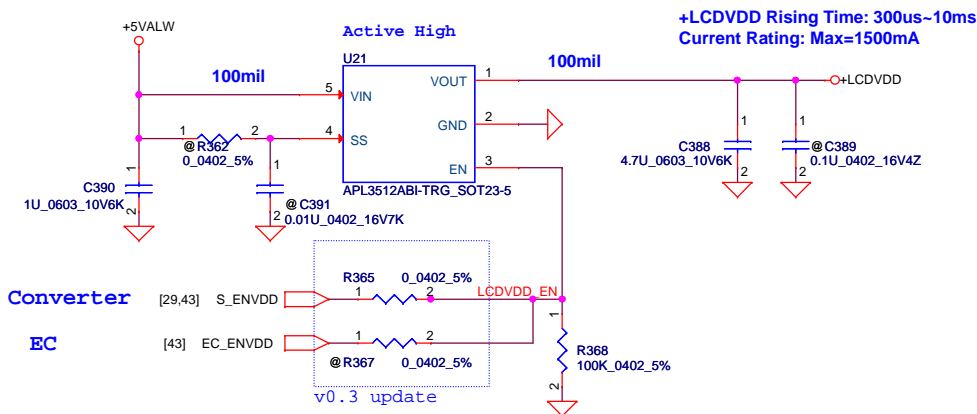
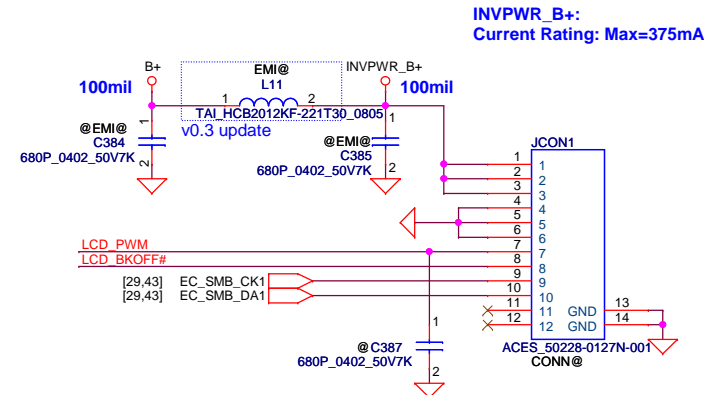
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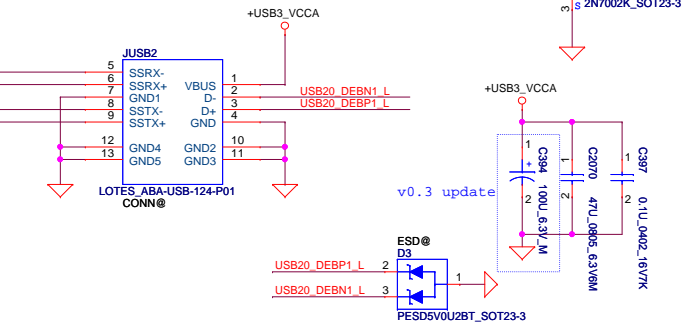
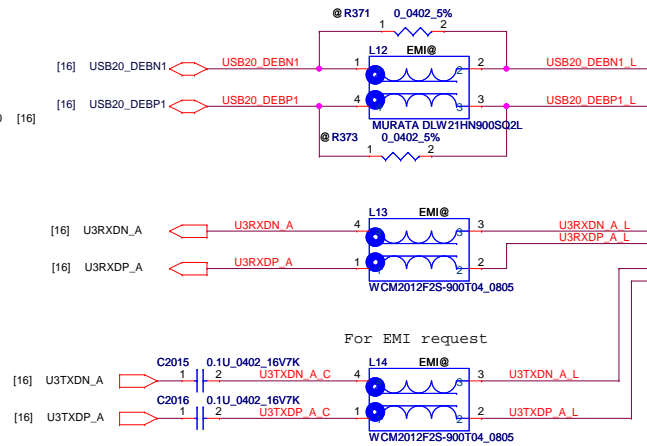
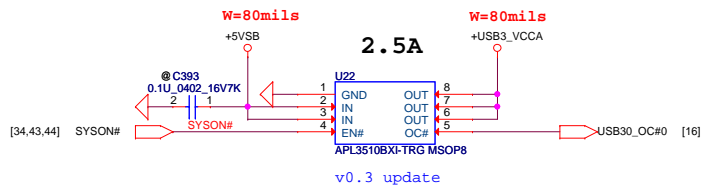
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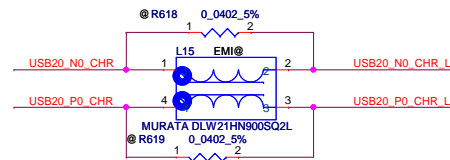
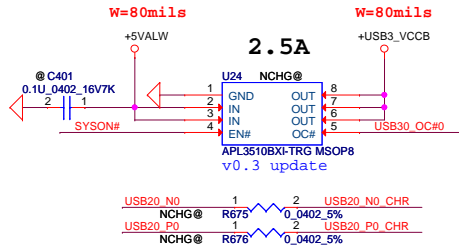
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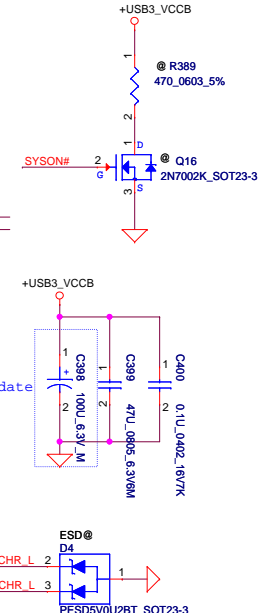
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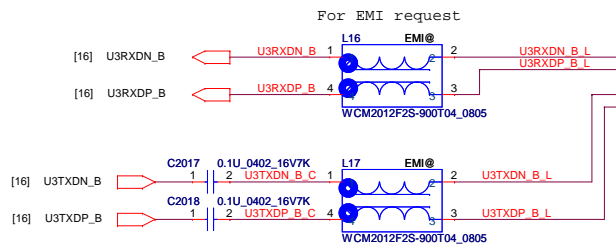
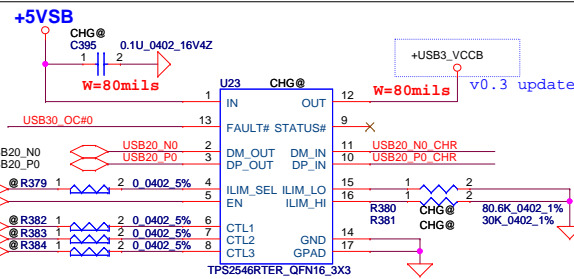
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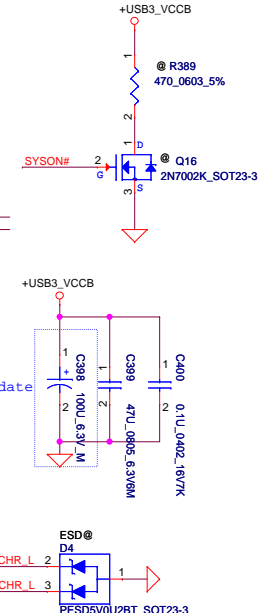
## Charge USB Port



## Charger

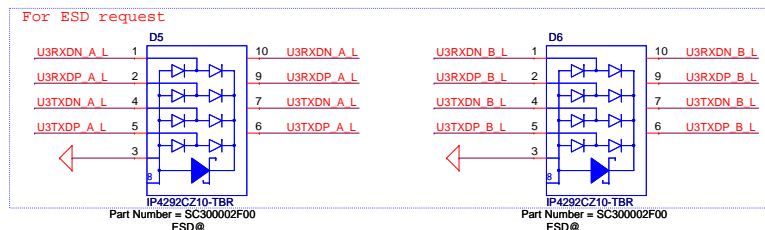


## Charge USB Port



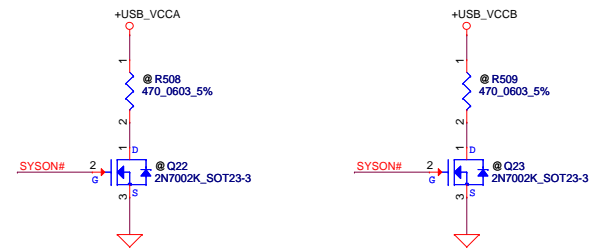
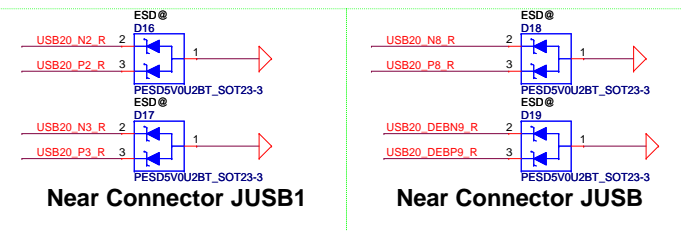
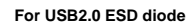
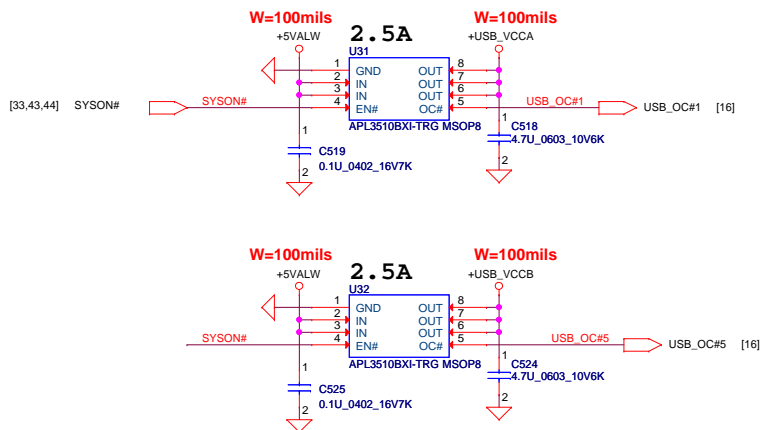
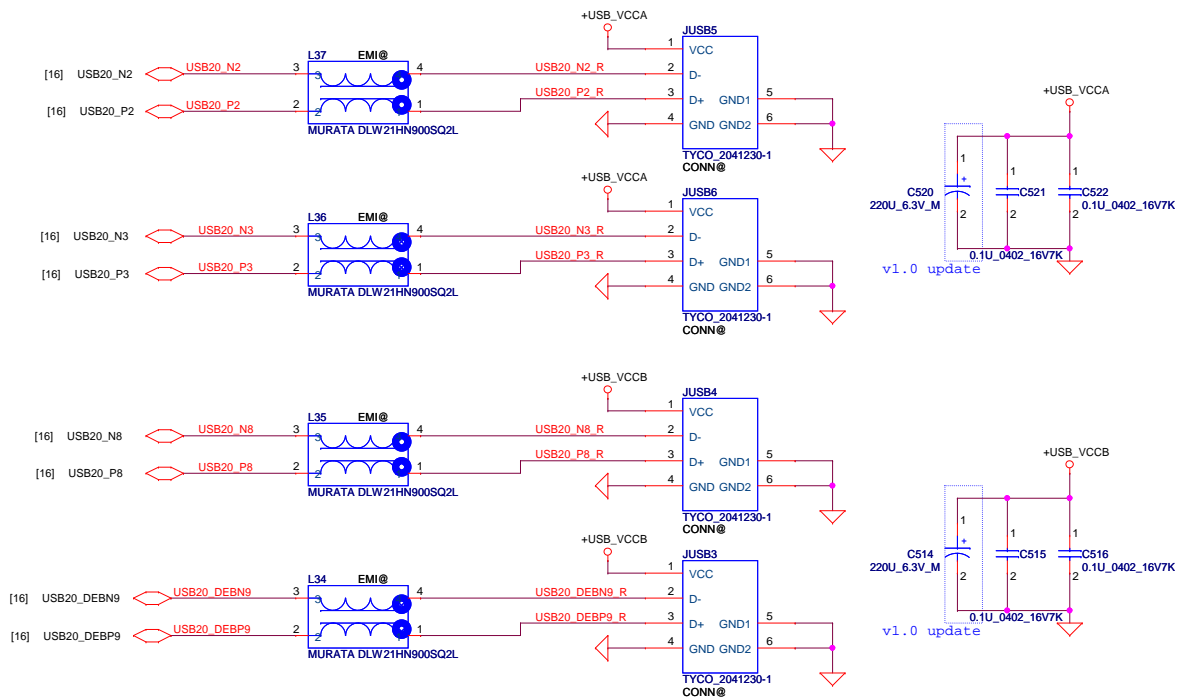
Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPIOA07(pin104)	GPIO22(pin41)	GPIOA11(pin108)	GPIO21(pin40)
S0 (CDP)	1	1	1	1
S3 (SDP)	1	1	1	1
S4/S5 (DCP)	0	0	1	1

System Global Power State	TPS2546/TPS2544 Mode	Charging	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP		1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs		1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake		0	0	1	1	ILIM_HI



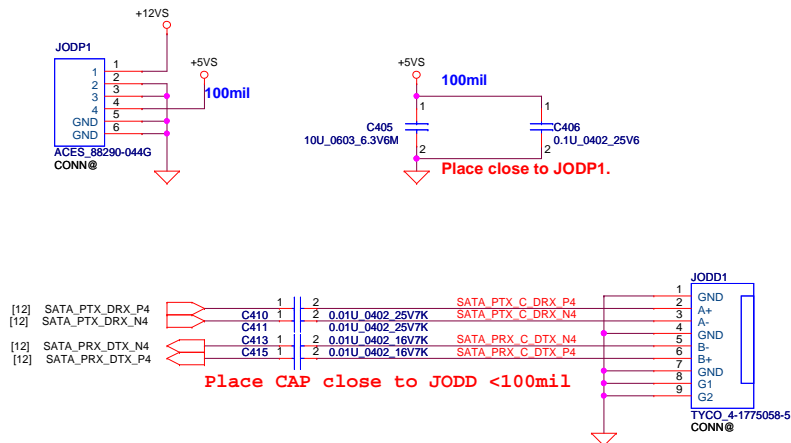
Security Classification	Compal Secret Data	Title
Issued Date	Deciphered Date	USB 3.0 CONN
Size	Document Number	Rev
Custom	ZEAO0 LA-A061P M/B	0.3
Date:	Sheet	33 of 59

# USB20

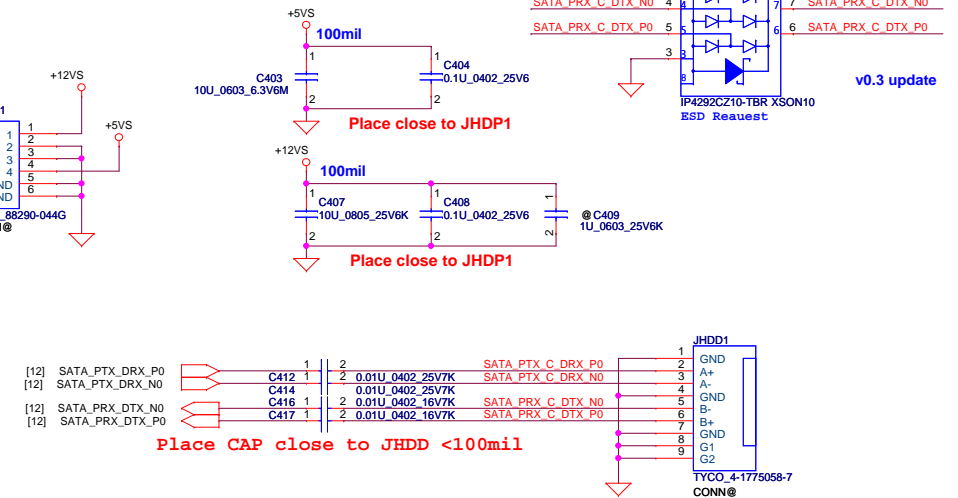


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				Date:	Tuesday, September 24, 2013
				Sheet	34 of 59

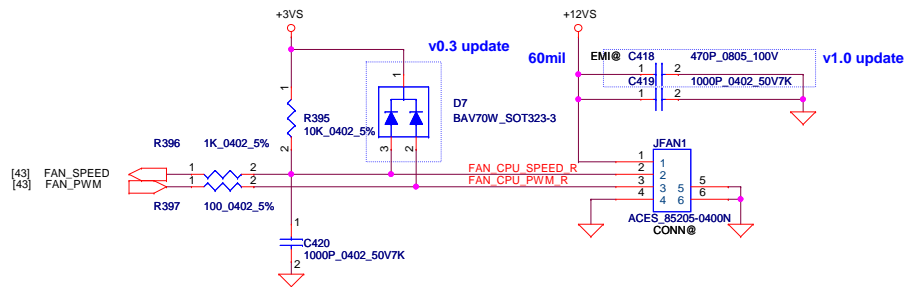
### SATA ODD Conn



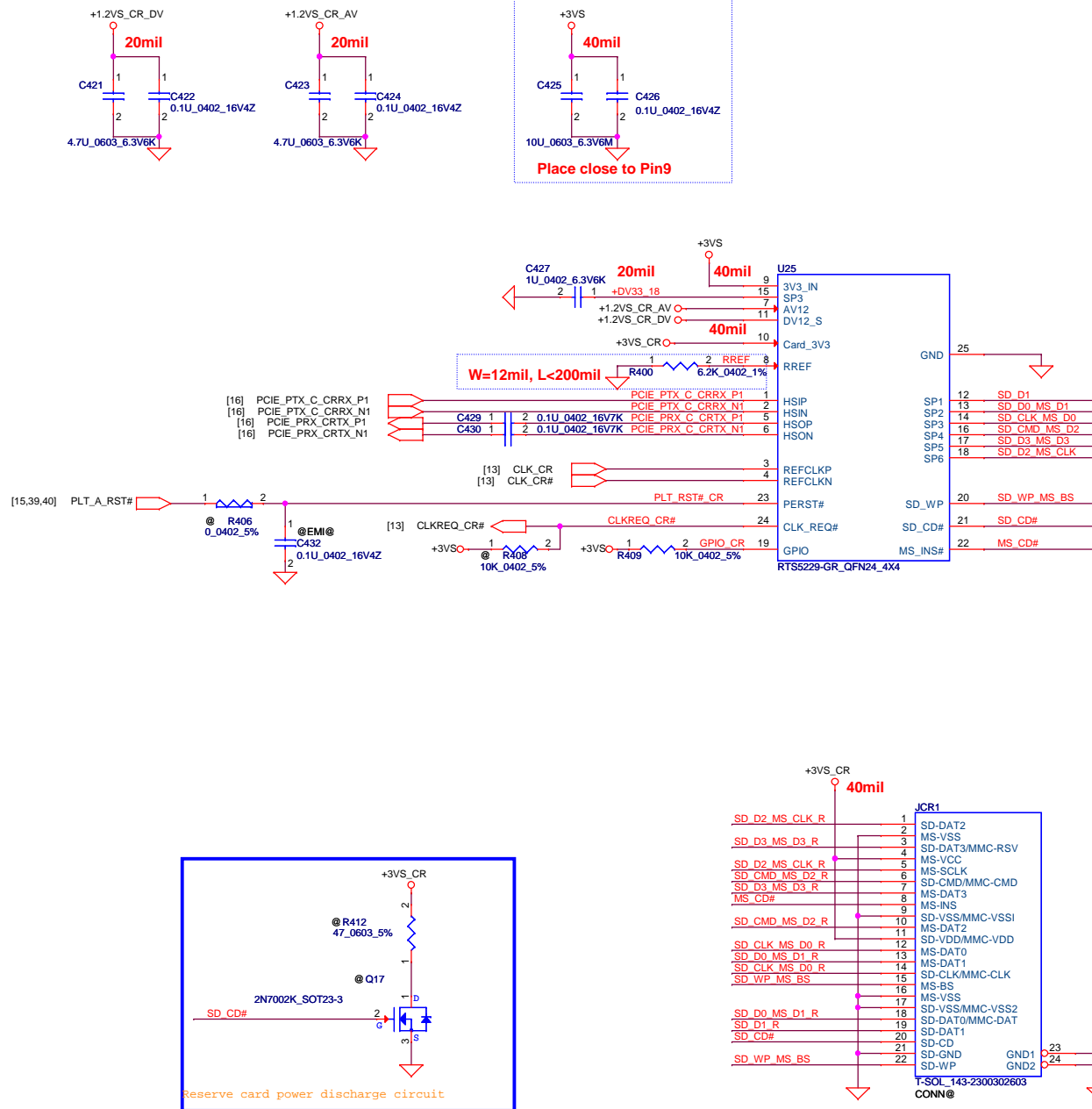
**SATA HDD Conn.**



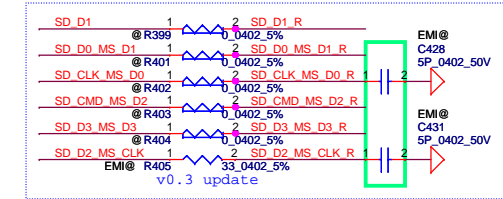
## FAN Control Circuit



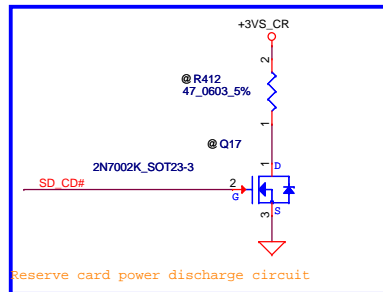
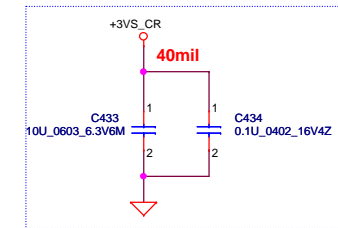
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title <b>SATA-HDD/ODD/USB</b>		
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					<b>ZEAO0 LA-A061P M/B</b>	0.3
				Date	Tuesday, September 24, 2013	Sheet



Length of per trace 2inch no more 2 via  
mismatch trace length <100mil  
50ohm +-15% impedance.



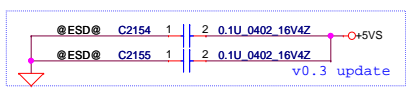
Place close to JCR1 pin 12,21



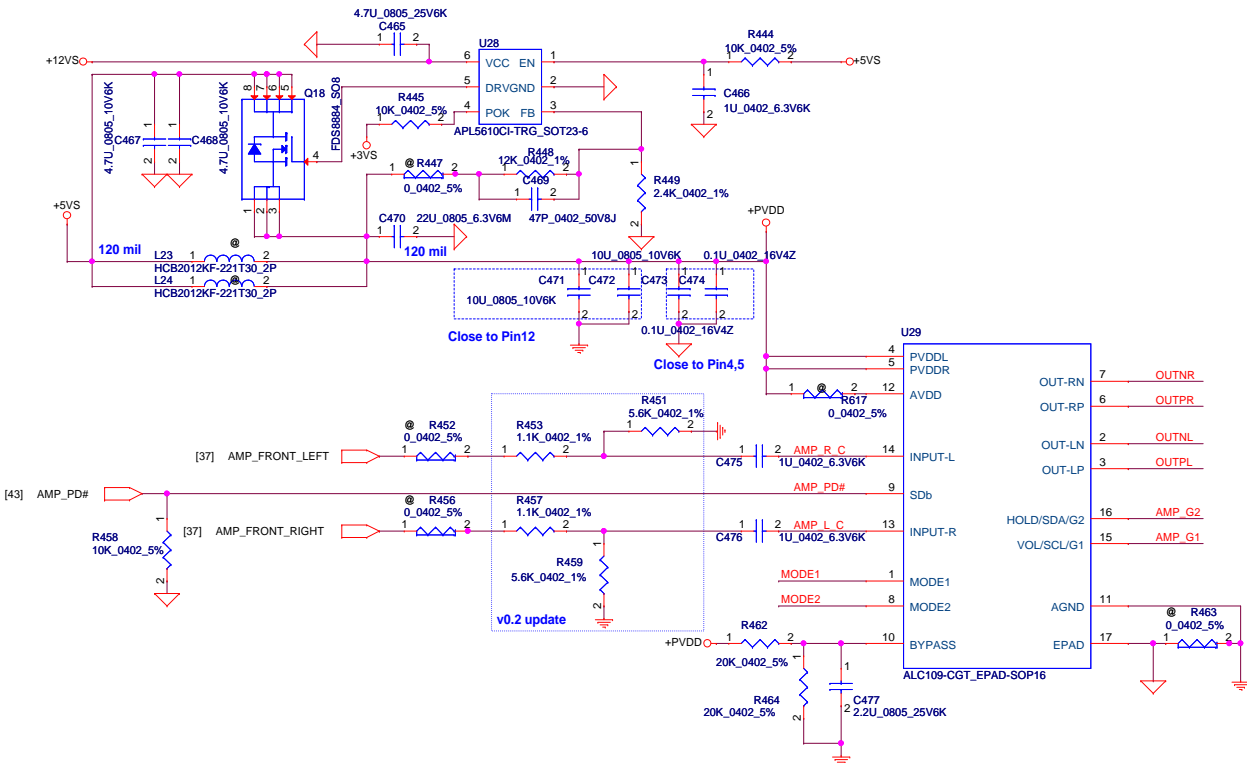
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Custom	0.3
				Date:	Tuesday, September 24, 2013
				Sheet	36 of 59



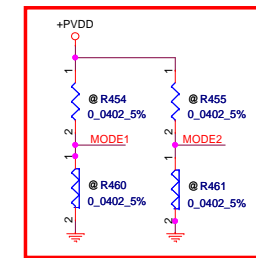




$V_o = 0.8(1 + R_{606}/R_{607})$   
Output: 4.8V  
Max I: 7.5A

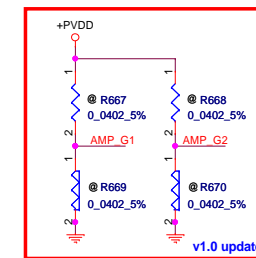


### Mode select: Fix Gain



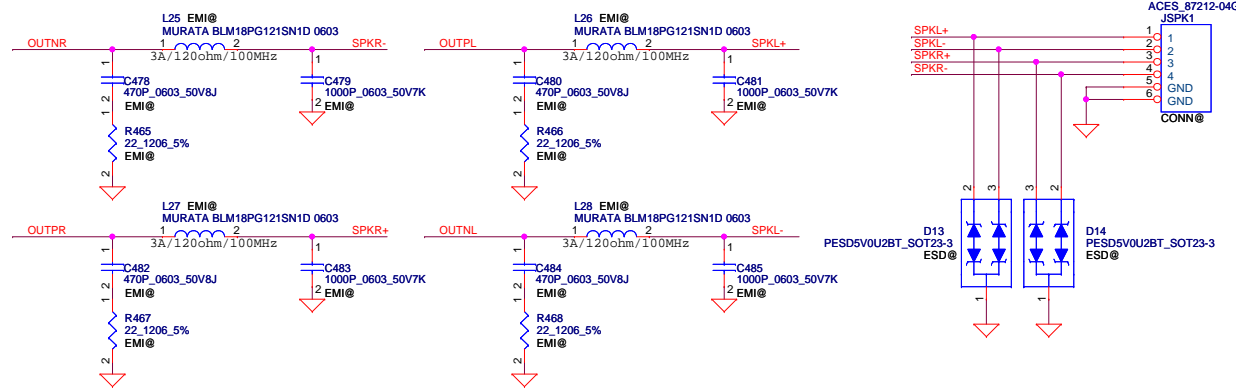
Model1	Model2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

### Gain Select



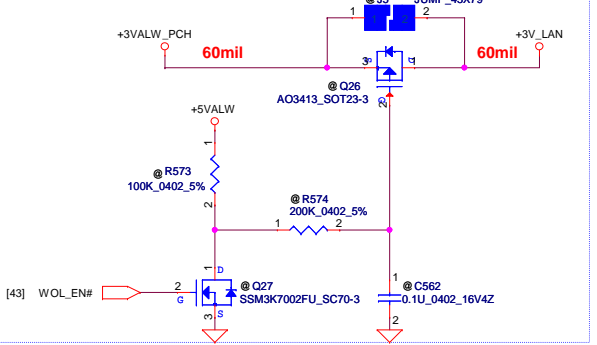
AMP_G1	AMP_G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

(Default)



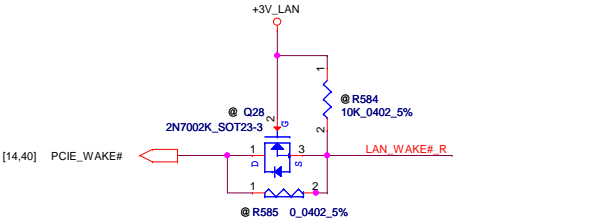
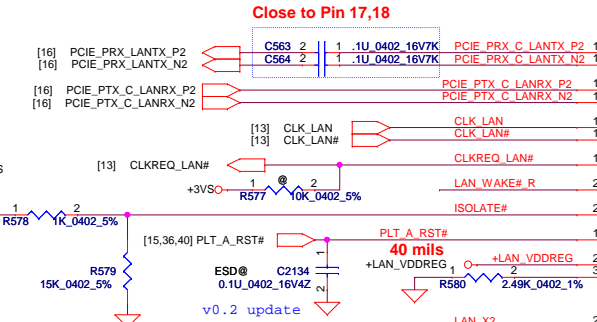
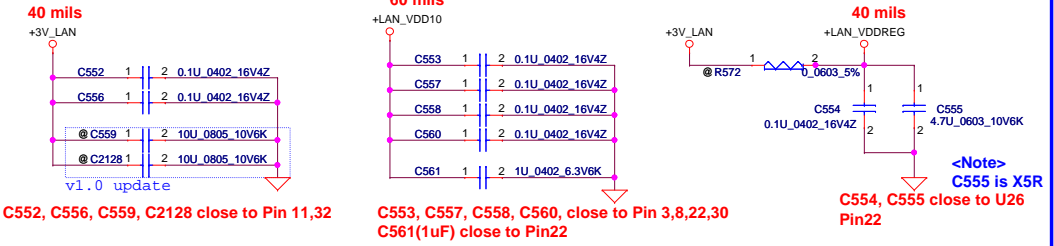
# WOL circuit

Short J5 for WOL support (Enable/Disable by BIOS setup)  
v0.2 update

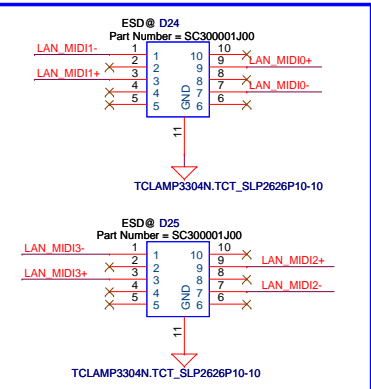
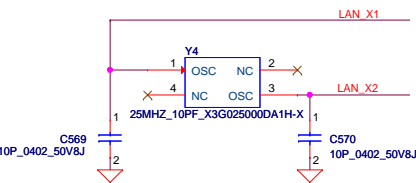


+3V\_LAN rising time (10%-90%) need > 0.5ms and <100ms.

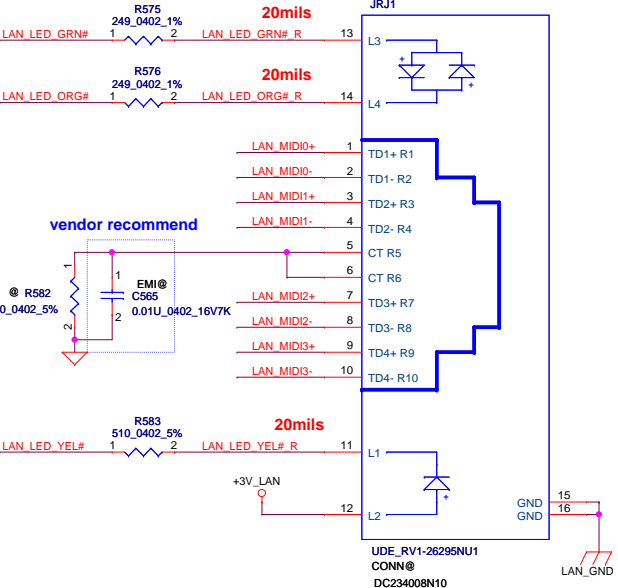
## Power ( Decoupling Cap. )



## Crystal



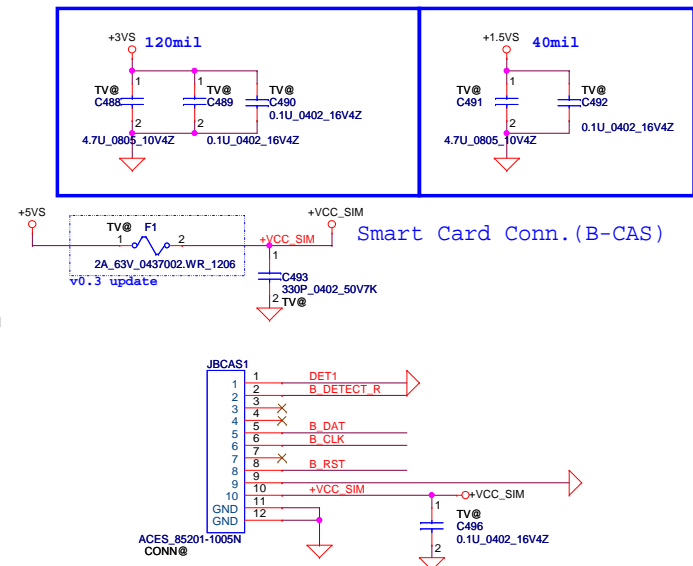
Green / Orage



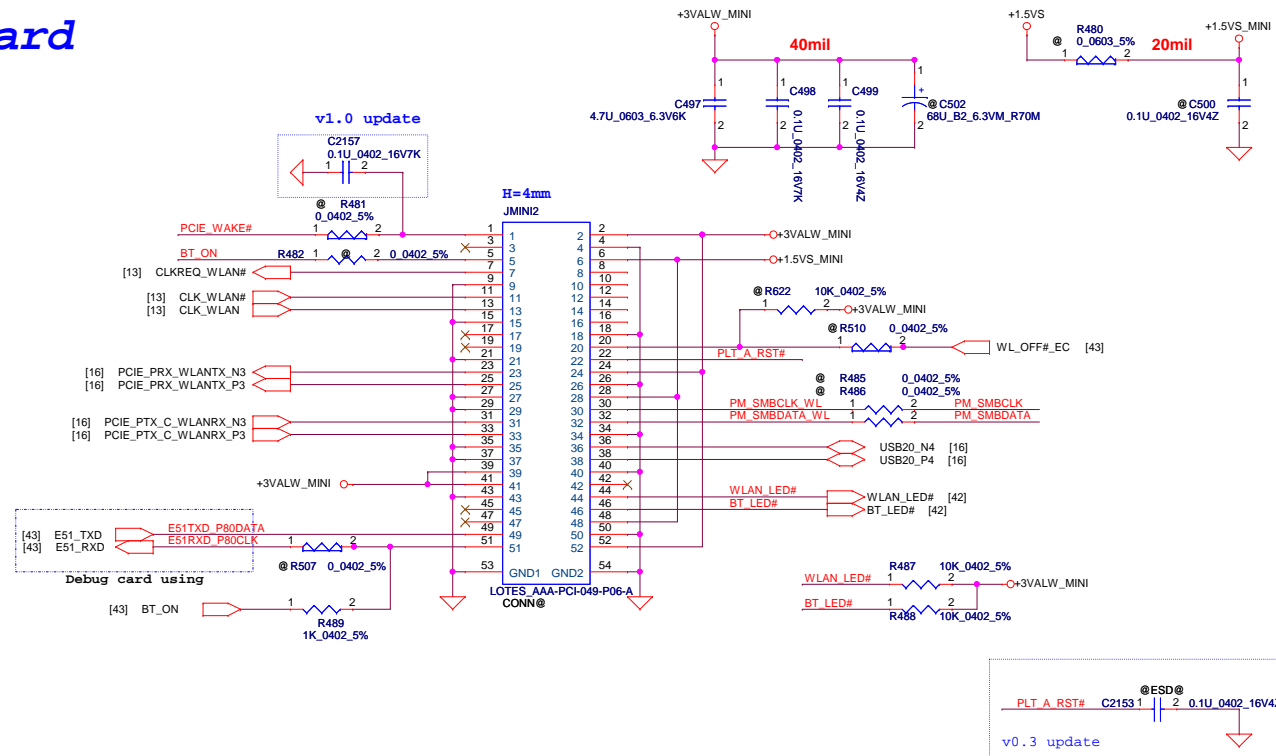
Yellow

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2013/04/01		2014/04/01		Rev	
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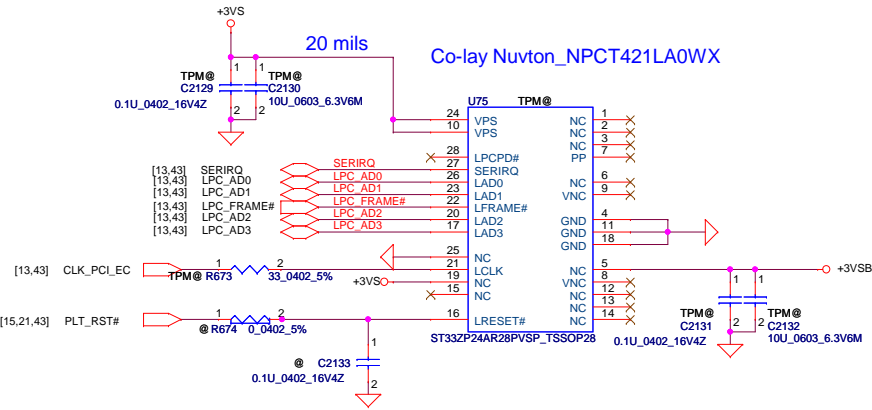
Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA



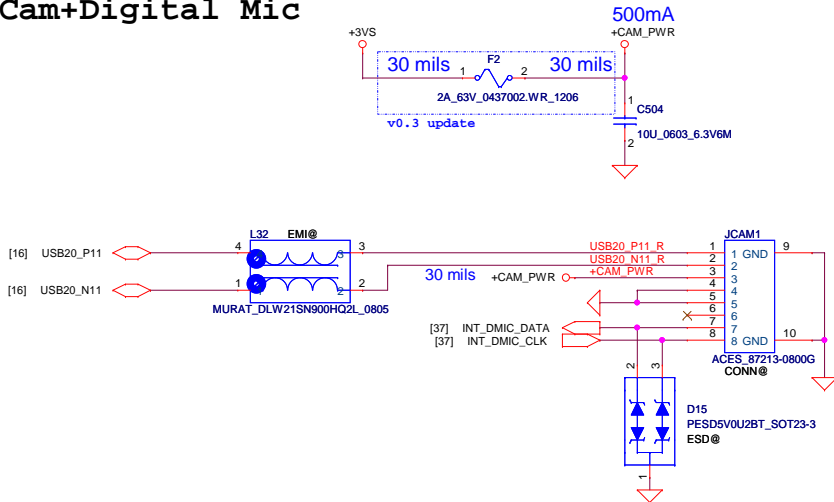
**Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,**



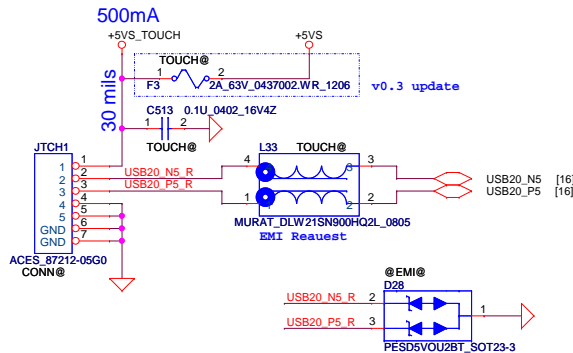
## TPM (Reserve)



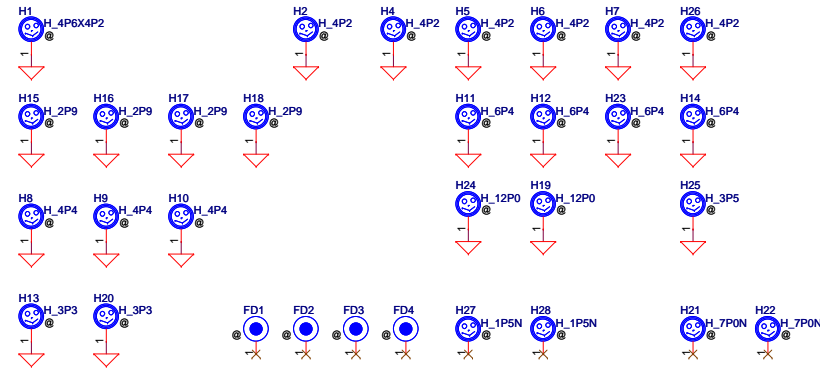
## WebCam+Digital Mic



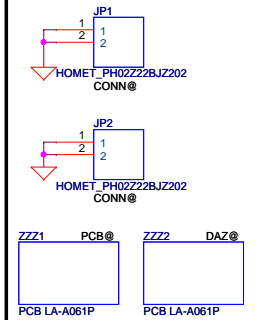
## Touch



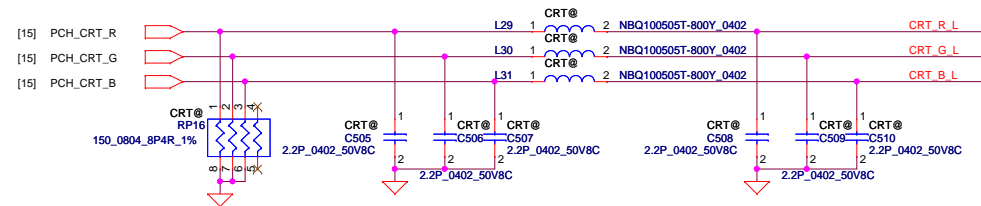
## Screw Hole



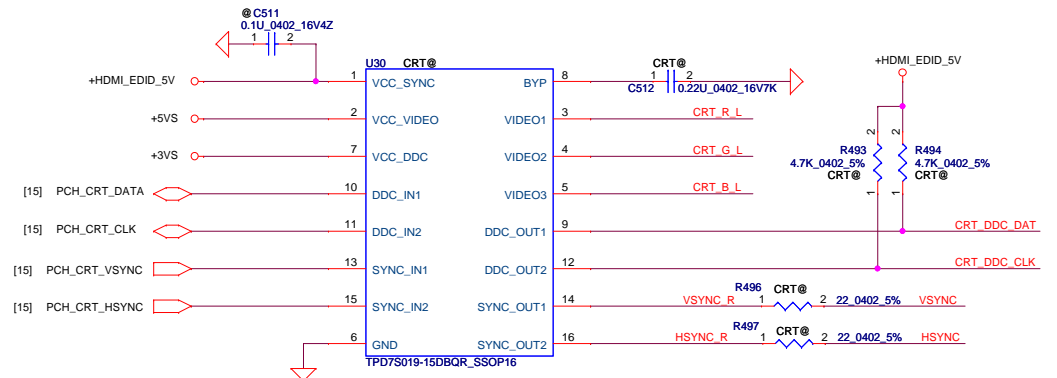
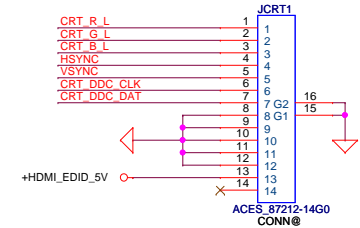
## PCH heat sink



## CRT Conn(Reserve 15pin)

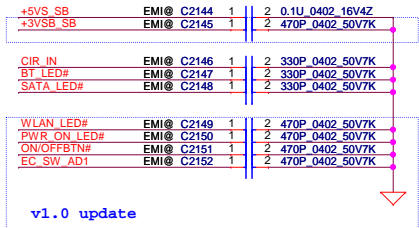


Need PU/PL on PCH/FCH side  
(2.2K\*2pcs for DDC & 150\_8P4R\*1pcs for RGB)



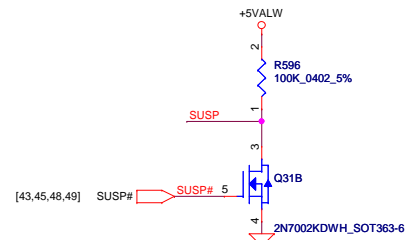
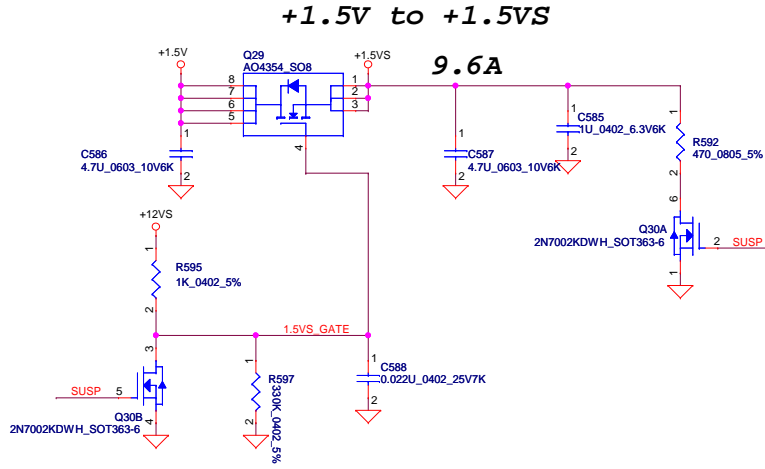
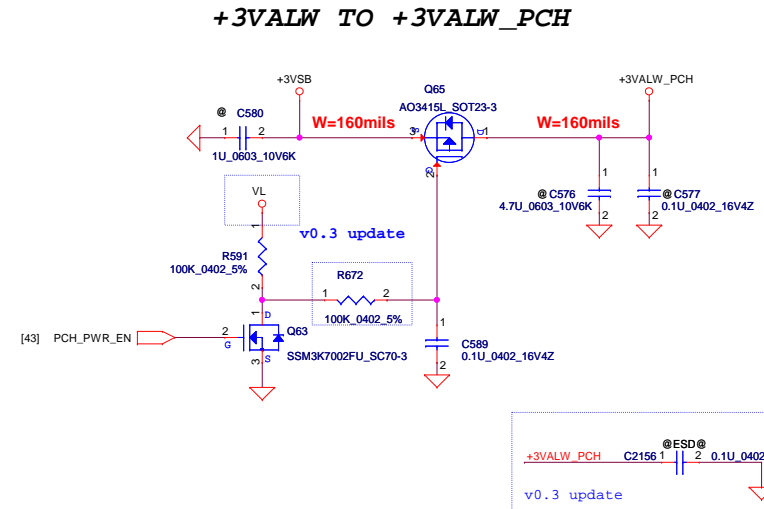
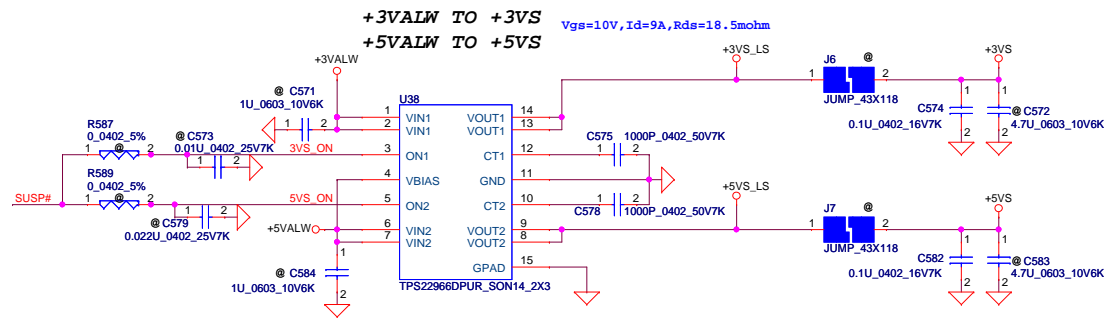
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PWR/Cap/TP/LED/LP/LS/Screw				
Size	Document Number	ZEA00 LA-A061P M/B		Rev 0.3
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### 8Pin sub-board Connctor

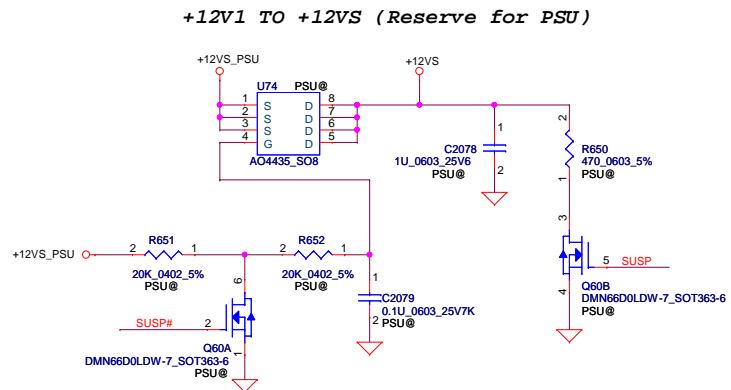
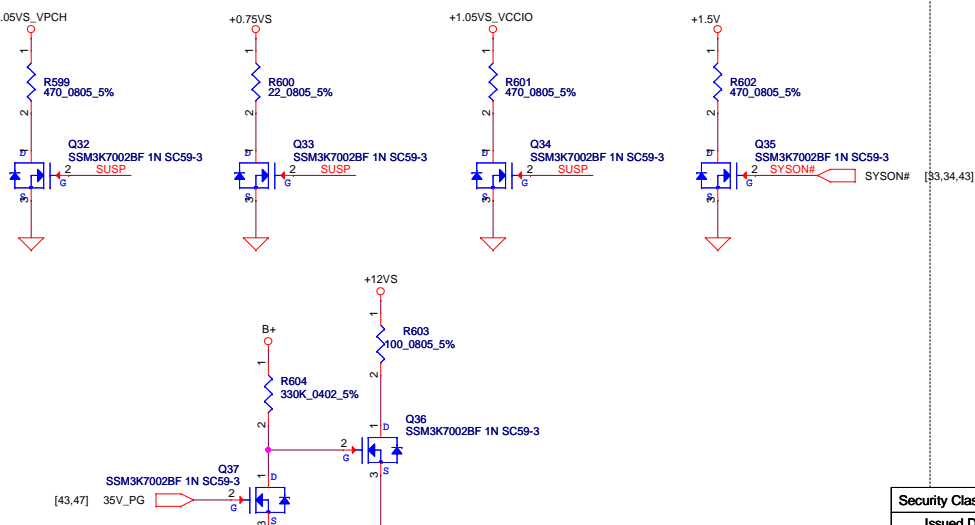






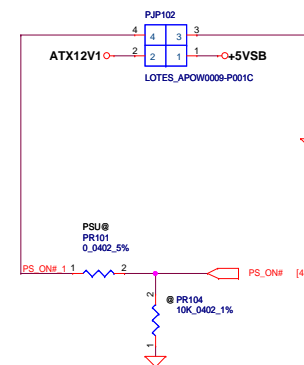
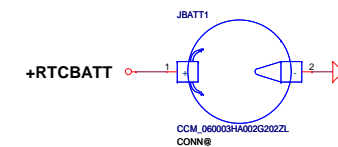


### Discharge circuit

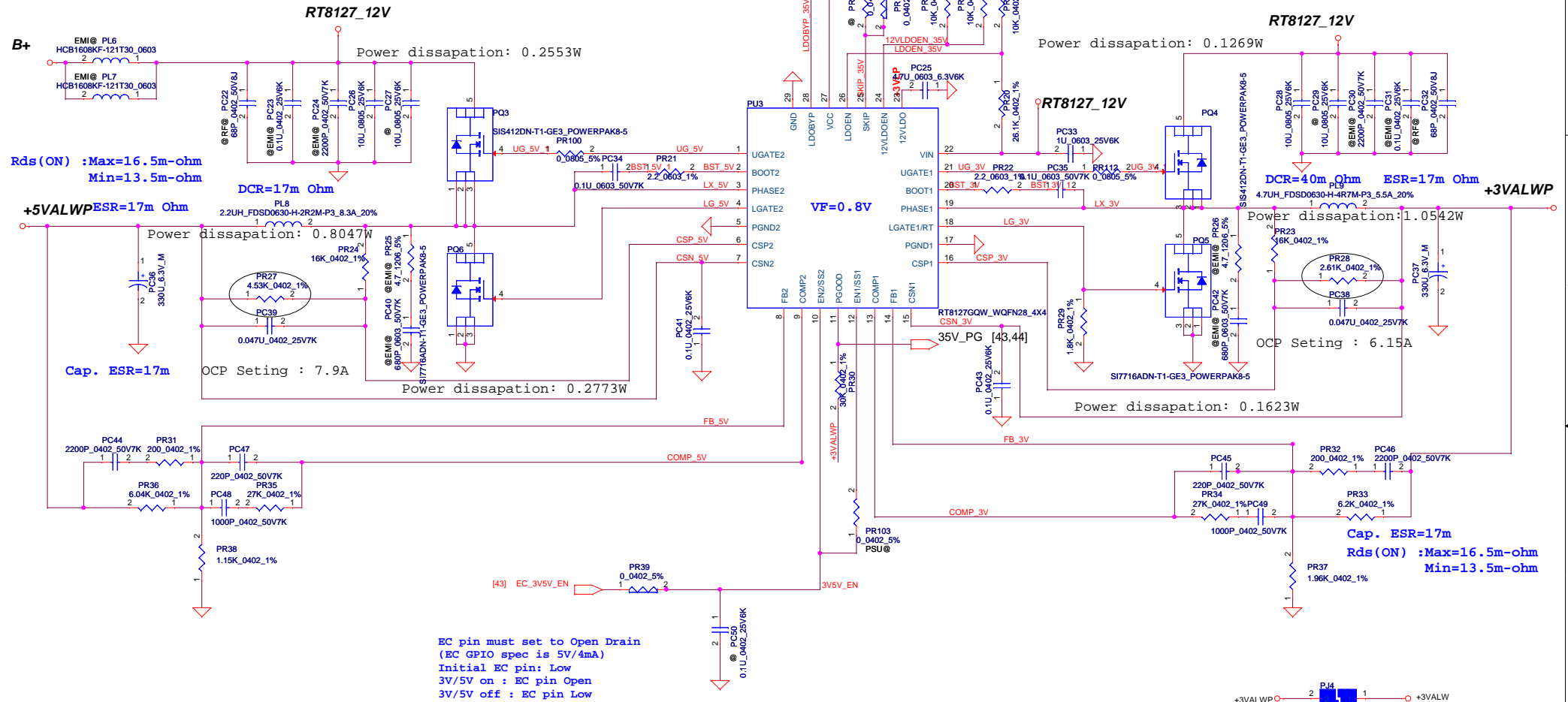


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ZEA00 LA-A061P M/B				Rev 0.3
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Ventura for CPU side  
slave address : 1000001  
please placemnet near R-sense



**+V\_5VP**  
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A  
Fsw=300K,  
Iocp>=8.66A  
Rds H/S --> typ:24 mohm ; max: 30 mohm  
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

**+V\_3.3VP**  
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A  
Fsw=300K  
Iocp>=5.33A  
Rds H/S --> typ:24 mohm ; max: 30 mohm  
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

TON (1)SMPS1=300KHZ (+5VALWP)  
(2)SMPS2=300KHZ (+3VALWP)

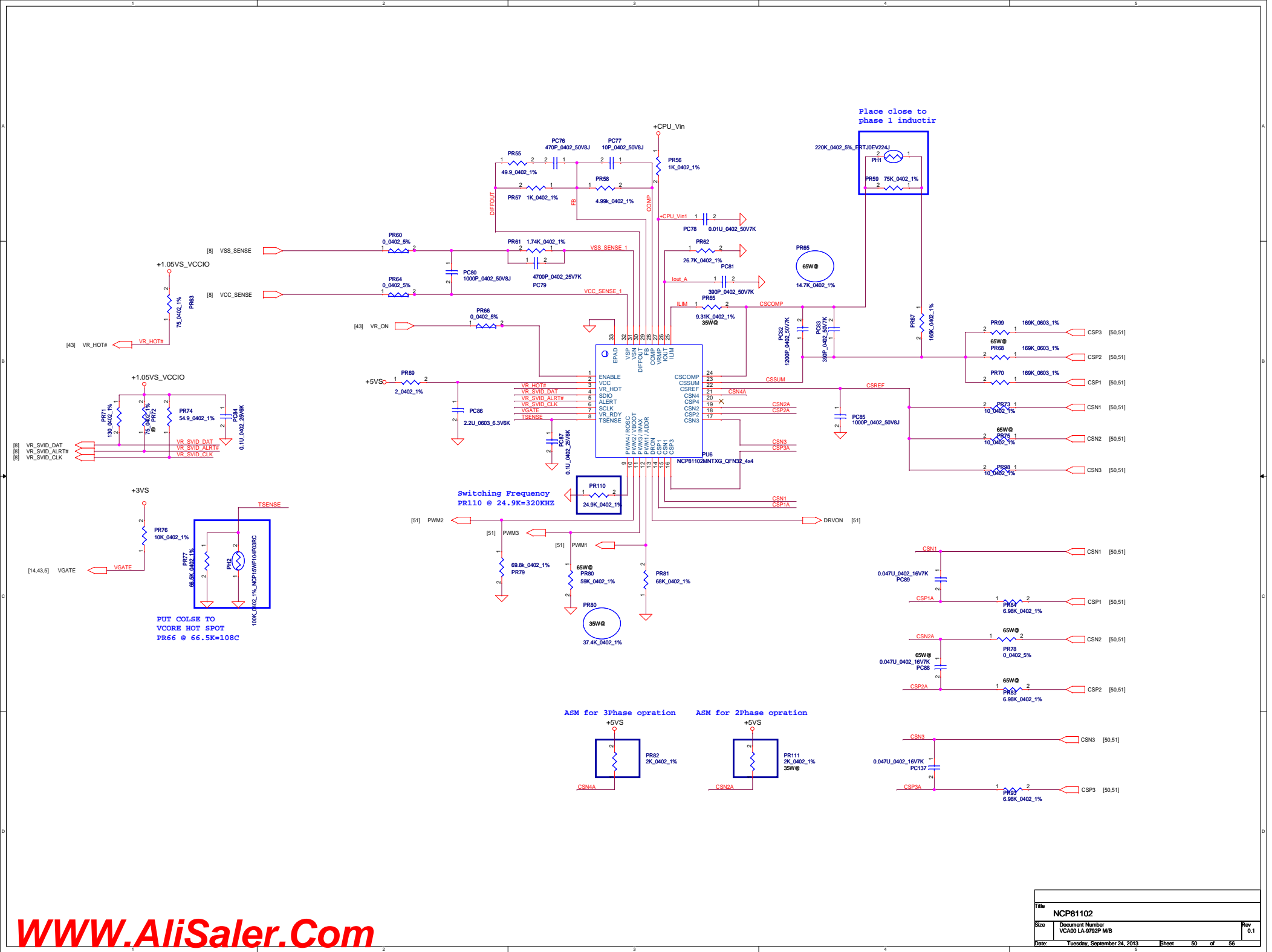
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Date: Tuesday, September 24, 2013				Sheet	47 of 56

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**PWR- 3VALWP/5VALWP**

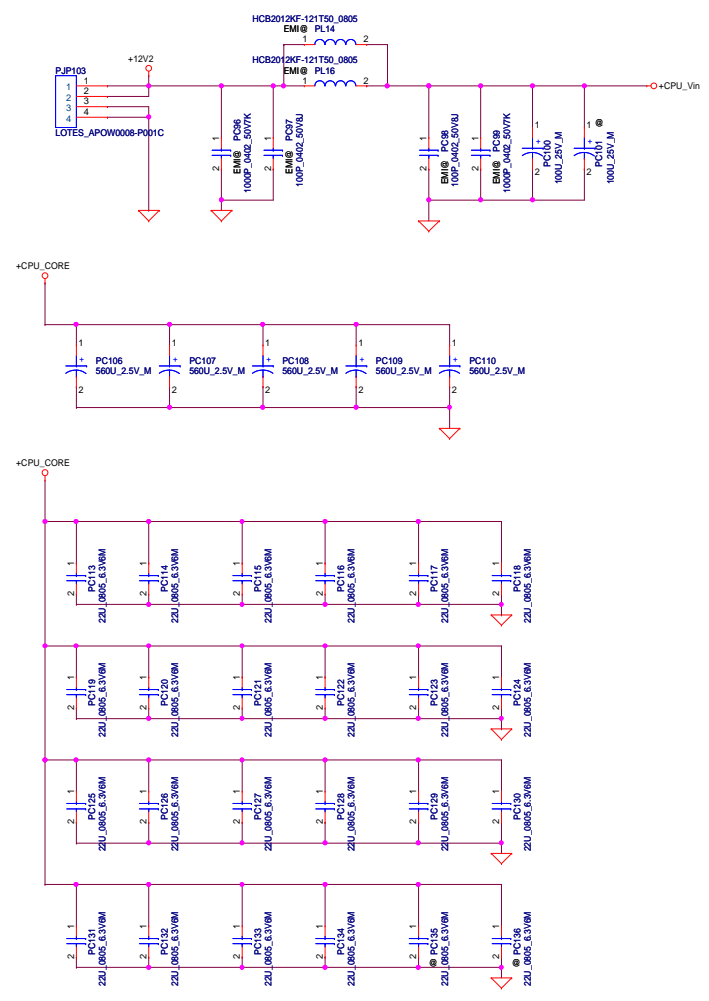
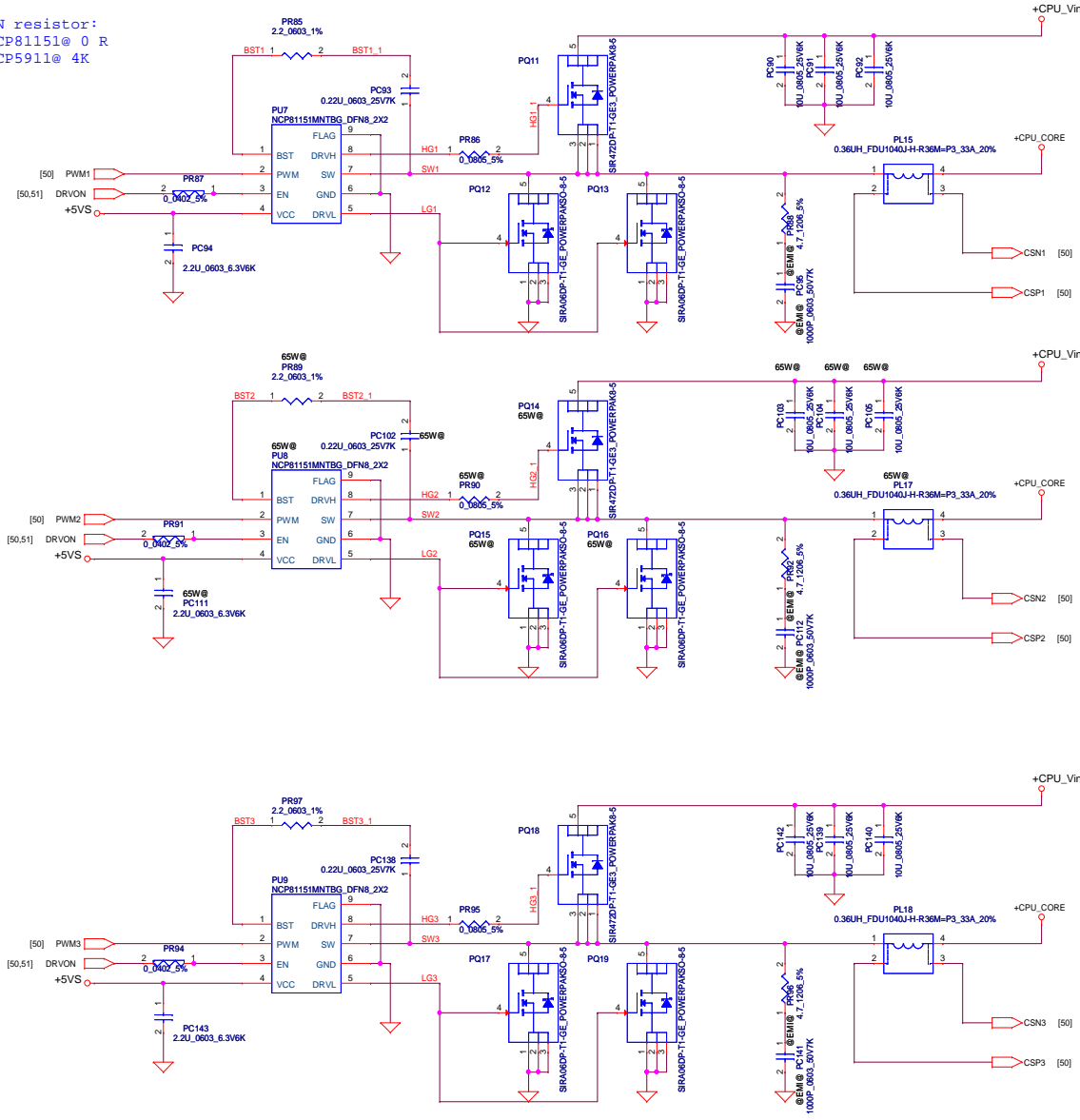




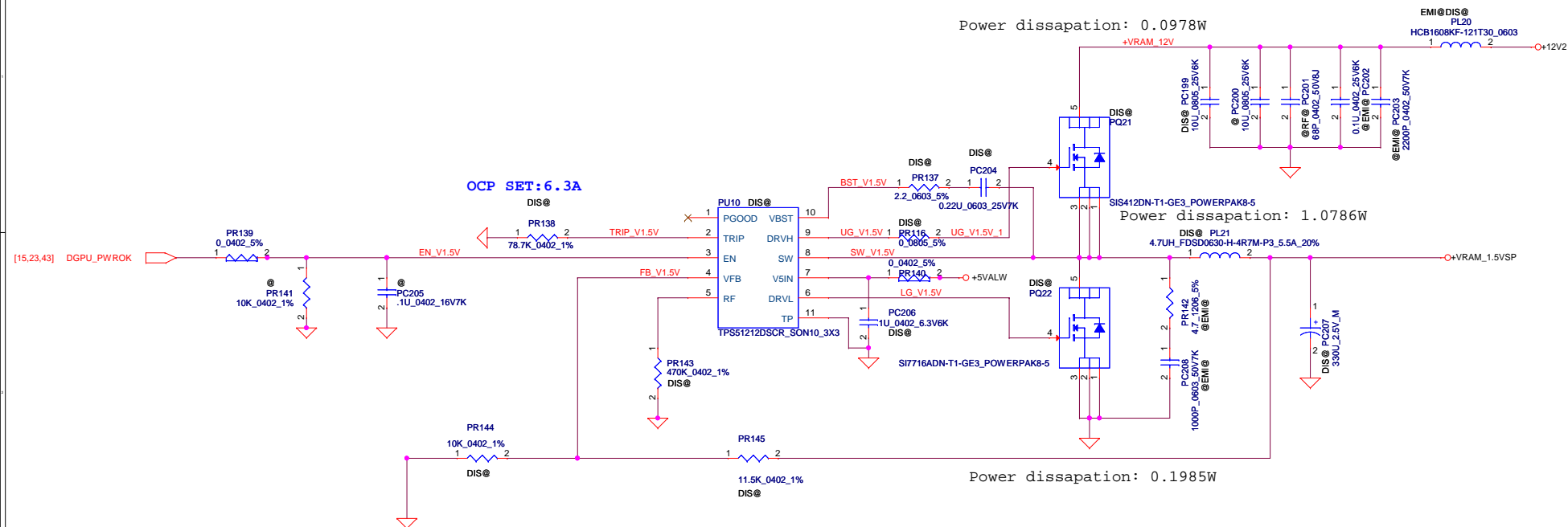




EN resistor:  
NCP81151@ 0 R  
NCP5911@ 4K





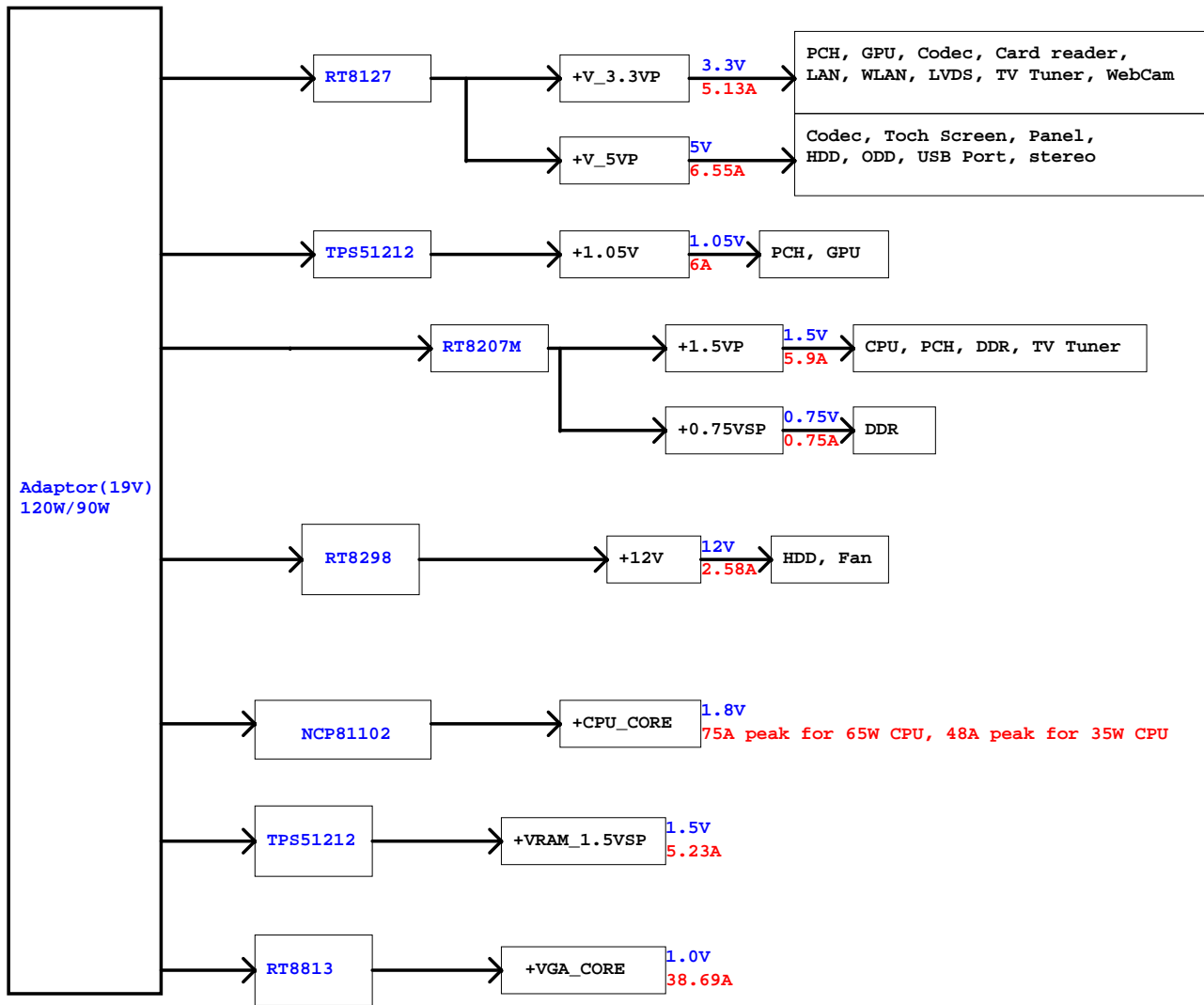


Cap. ESR=17m  
 Rds(ON) :Max=15m-ohm  
 Typ=12m-ohm  
 Vtrip range ==> 0.2V ~ 3V  
 <Vo=1.5V> VFB=0.7V  
 V=0.7\*(1+11.5K/10K)=1.505V  
 Fsw=290KHz

Ipeak=4.7A, Imax=3.29A, Iocp=1.2\*Ipeak=5.64A

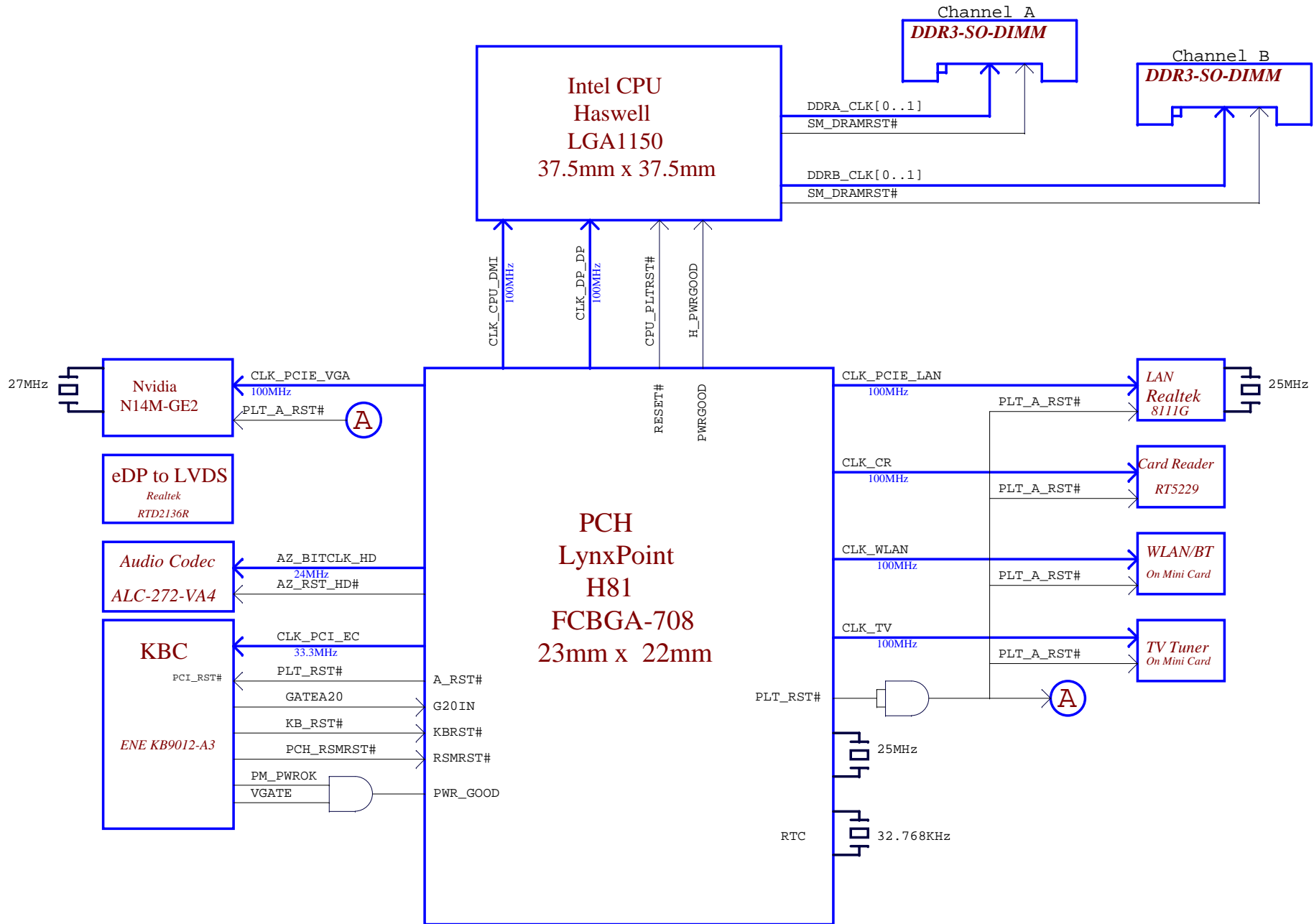
Iocp(set)=5.718A~8.304A

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								Size		Document Number		Rev	
								Custom		VCA00 LA-9792P M/B		0.1	
								Date:		Tuesday, September 24, 2013		Sheet 53 of 56	

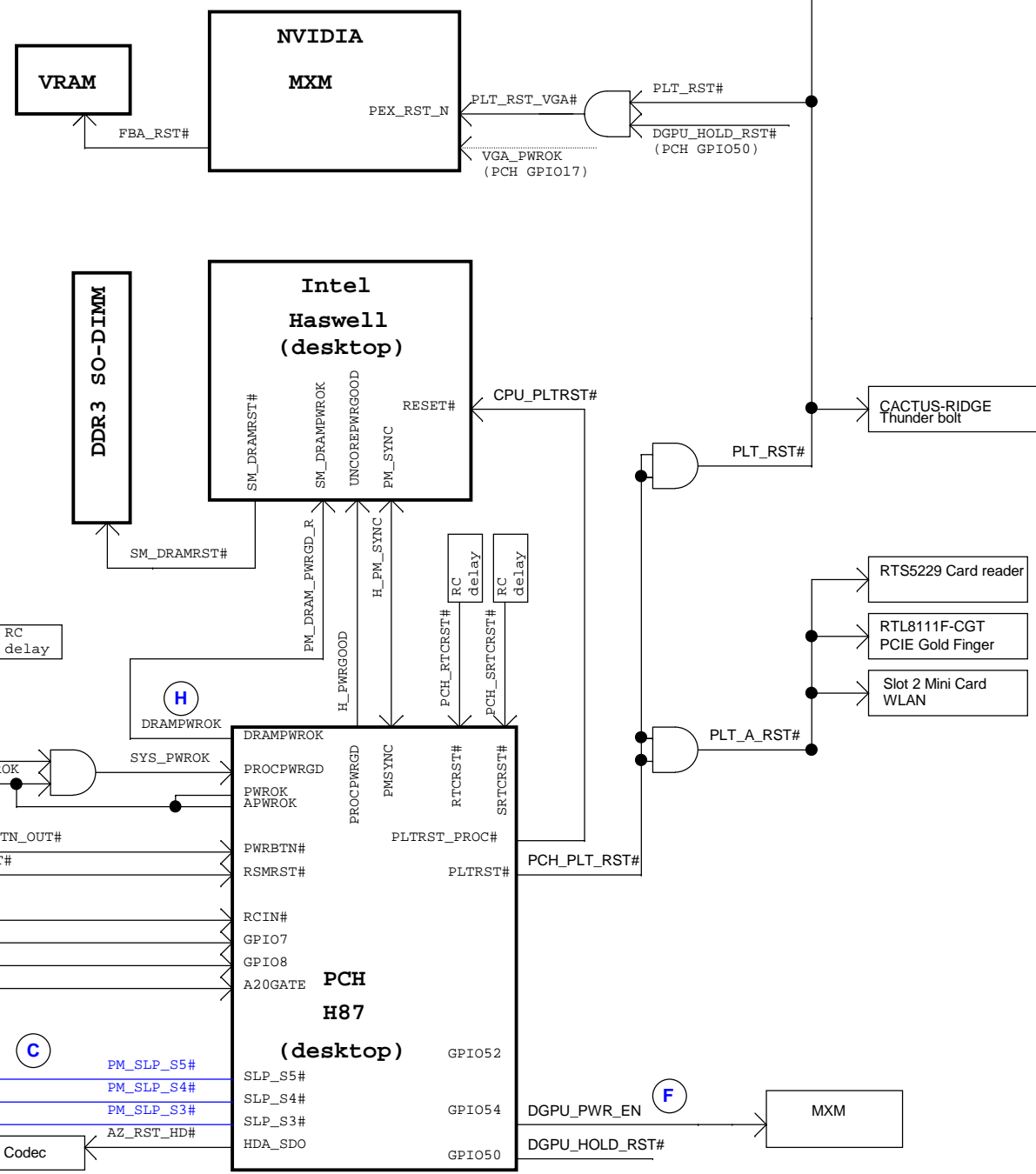
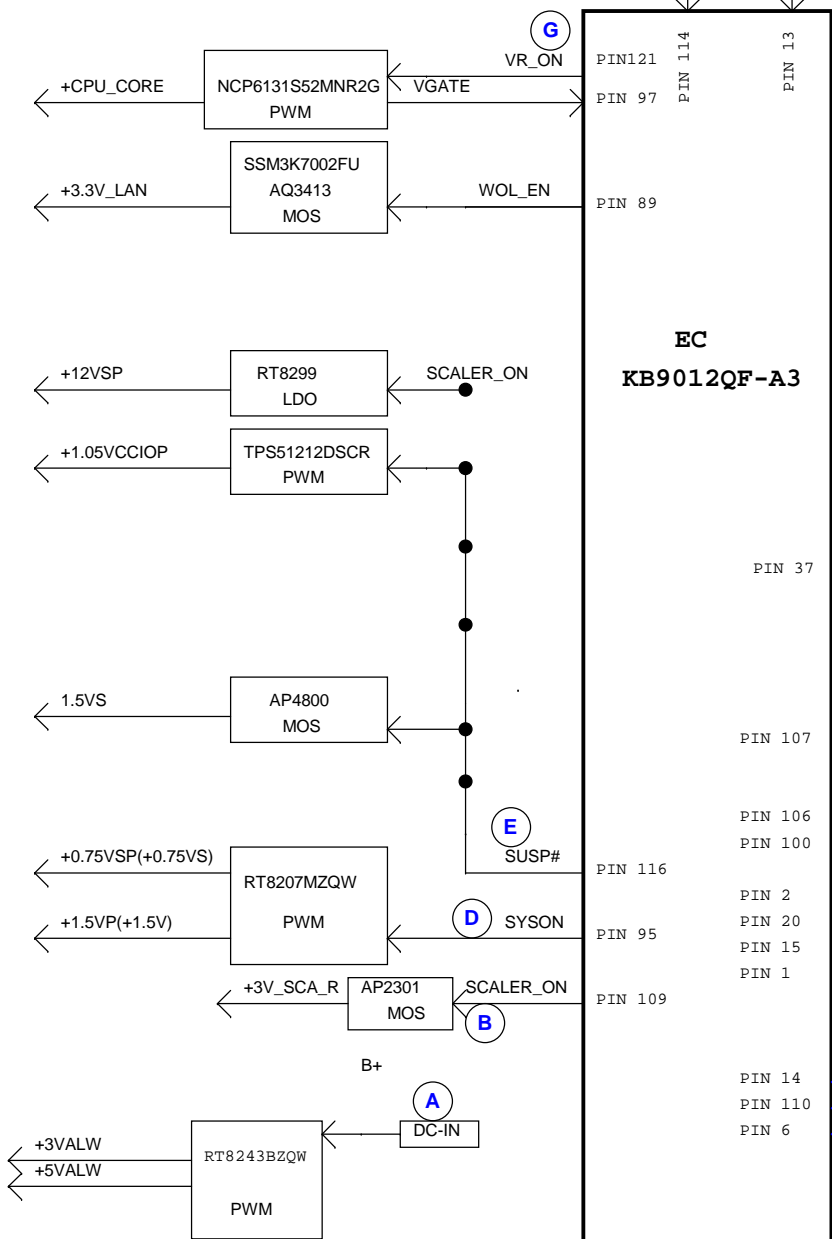
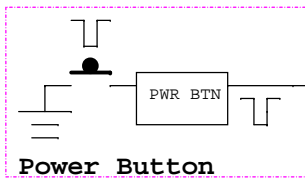


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/09/12	Deciphered Date	2012/09/12	Title	Power Rail
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				Date: Tuesday, September 24, 2013	Sheet 55 of 59

# Clock and Reset Diagram



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				Clock/Reset Diagram
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				Rev 0.3
				Date: Tuesday, September 24, 2013 Sheet 56 of 59



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NO.	DATE	PAGE	MODIFICATION LIST	REASON
1.	20180604	F47	Add F47A and Change the p.JCI to S400002A600	For Pericran Issue
2.	20180720	F47	Add F47C2, F47C22, S47C2	For PMU Request
3.	20180720	F47	Add F47	For PMU Request
4.	20180720	F47	Add F47C	For SC driver Issue



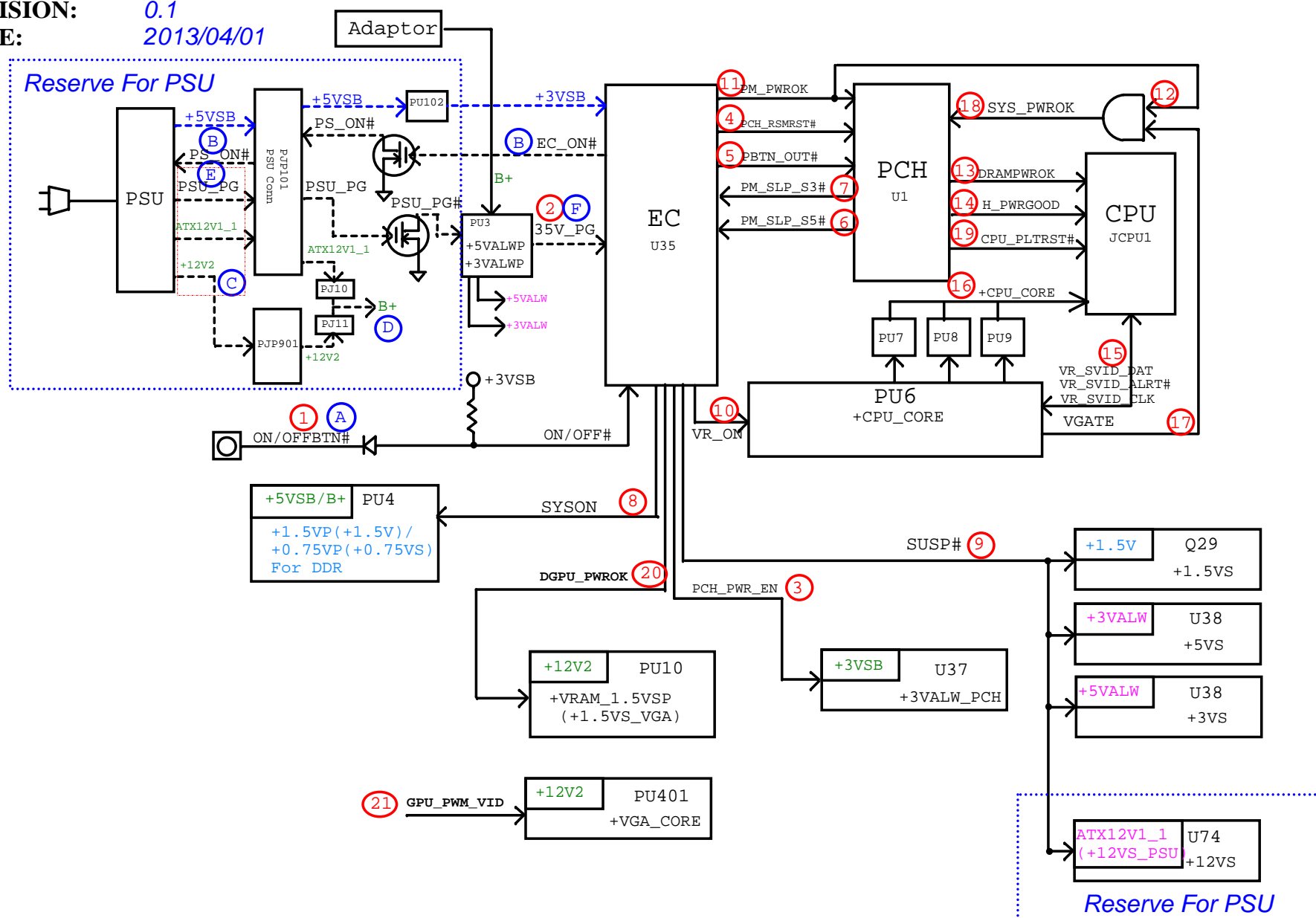
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**MODEL NAME:** *ZEA00 Power Sequence Block Diagram (Discrete)*

PCB NAME: LA-A061P

REVISION: 0.1

DATE: 2013/04/01



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HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 --> 0.2

GERBER-OUT DATE: 2013/06/20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.			Change C45 from SF000002V00 to SF000003X00	
2.			Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.	
3.			<del>Change LCD_RKOFF# control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.</del>	
4.			Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.	
5.			Pop R428 for AZ_SDIN0_HD.	
6.			U2 footprint change from socket to IC.	
7.			Add RH11	
8.			Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF	
9.			Change R423 location to L45	
10.			Change D7 from SC2N202U010 to SC600000B00 for 替代料	
11.			Change Q29 from SB548000210 to SB000002N00.	
12.			Change D8&D9 from SCS00002G00 to SCS00000Z00	
13.			X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB000000E000. 2.Change Q9 from SB934130020 to SB934130000. 3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.	
14.			Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.	
15.			Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).	
16.			Change Q10 from SB00000FC00 to SB00000L800 for 替代料	
17.			Remove R469 0ohm for TV.	
18.			Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.	
19.			Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.	
20.			Pop U7&R231, un-pop R228 for PLT_RST_VGA#.	
21.			Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.	
22.			Un-pop LAN power components Q26,Q27,R573,R574,C562.	
23.			0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647	
24.			Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.	
25.			Pop R438,R439 for ESD request.	

PVT change list:

- Change Q10 from SB00000FC00(EOL soon) to SB000002N00(同Q29),SB00000FC00 as 2nd source.Schematic, 平衡滤波
- Change U23 pin12\_+USB3\_VCCA to +USB3\_VCCB, pop U22, un-pop U24 for USB charger
- R365 change from short pad to 0ohm.
- U5 pin5 change from +3VS to +3VALW\_PCH for BCM43142 wake from WLAN issue.
- Change R473,R490,R677,R678,R679 from SP040005X00\_0603 size to F1,F2,F4,F5,F3 SP040003S00\_1206 size.
- Change L11 from SM010014520 to SM01000EJ00 for ACL request
- Change L8 from SM010007W00 to SM010019400 for ACL request
- Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
- Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
- Change R276 from 10k to 100k for +3VS\_VGA rise time.
- Change R672 from 10k to 100k for +3VALW\_PCH rise time.
- Change R438 & R439 from 0\_0603 to short pad.
- Un-pop C125 & C548 for sequence EA.
- Change C394, C398,C520 & C514 from 220uF(LELON\_SF000001F00) to 100uF (Panasonic\_SF000005100) to meet Inrush EA & ACL request.
- Change C170 & C171 from 12pF to 10pF for EA.
- Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
- Add R677 & reserve R678 on U5 AND gate for PLT\_A\_RST#
- Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
- Change R591 pull-high from +5VSB to VL for power S5 Erp request.
- Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
- Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
- Add C2144-C2152 for EMI request.
- Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
- Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
- Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
- Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

pre-MP change list:

- Change R399,R401,R402,R403,R404 from 0ohm to short pad.
- Add C2157 and reserve C2158.
- Change R8,R470,R669,R670,R416 from 0ohm to short pad.
- Un-pop JECDB1 & SW1.
- For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
- Change C520 & C514 from 100uF to 220uF.
- Pop C2149-C2152 for ESD request.
- Change C559 & C2128 from 0603 to 0805.
- Change C2145 from 0.1uF to 470pF, change C2149-C2152 from 330pF to 470pF for EMI.
- Add C418 for EMI.

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